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# MS-7C75

## CML Platform

ATX  
Ver: 1.1

### CPU:

*Comet lake S 65W*

### Onboard Chip:

*HD Audio Codec:ALC892*

*LAN-RTL8125B*

*SIO:NTC6687*

*Flash ROM: SPI 128 MB X1*

### Main Memory:

*DDRIV (2666MHz) \* 4 (Dual Channel)*

### ACPI:

*LDO*

### Expansion Slots:

*PCI Express (X16) Slot \* 1*

*PCI Express (X4) Slot \* 1*

*PCI Express (X1) Slot \* 3*

*M.2 Slot \* 2*

### System Chipset:

*Z490 PCH\_H*

### VGA Output:

*HDMI Port*

*DP Port*

### PWM:

*IMVP8 -RT3609BE*

### Other:

*SATA3.0 \*6*

*USB2.0 \*6*

*REAL USB3.1 Gen2 Type A+C*

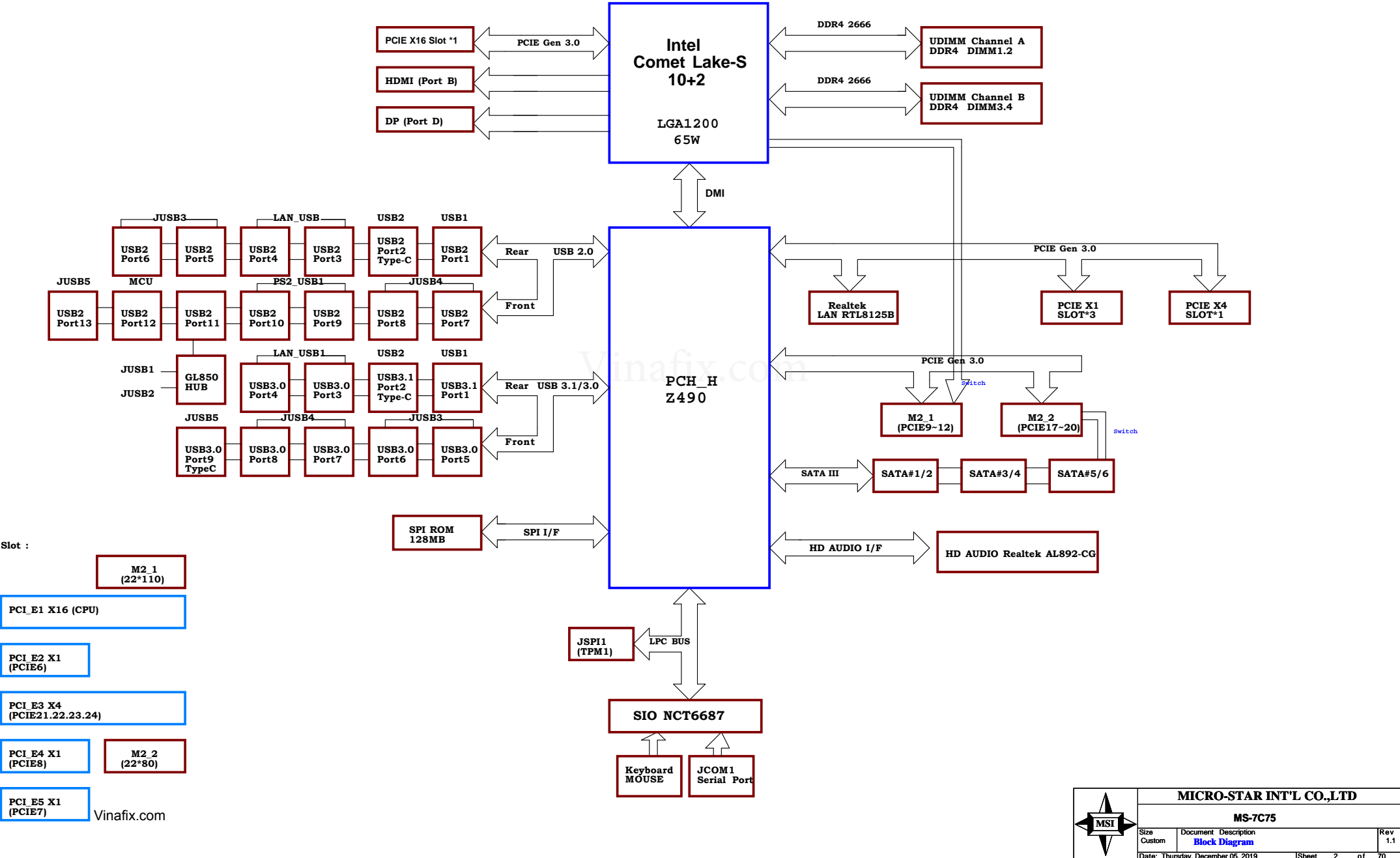
*REAL USB3.1 Gen1 LAN\_USB*

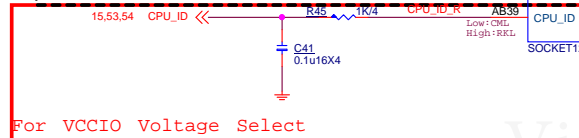
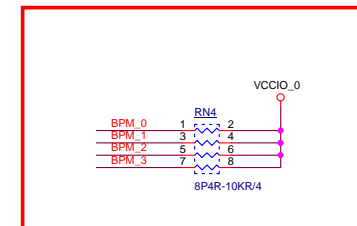
*FRONT USB3.1 GEN1 TypeC*


*FRONT USB3.0 \*4*

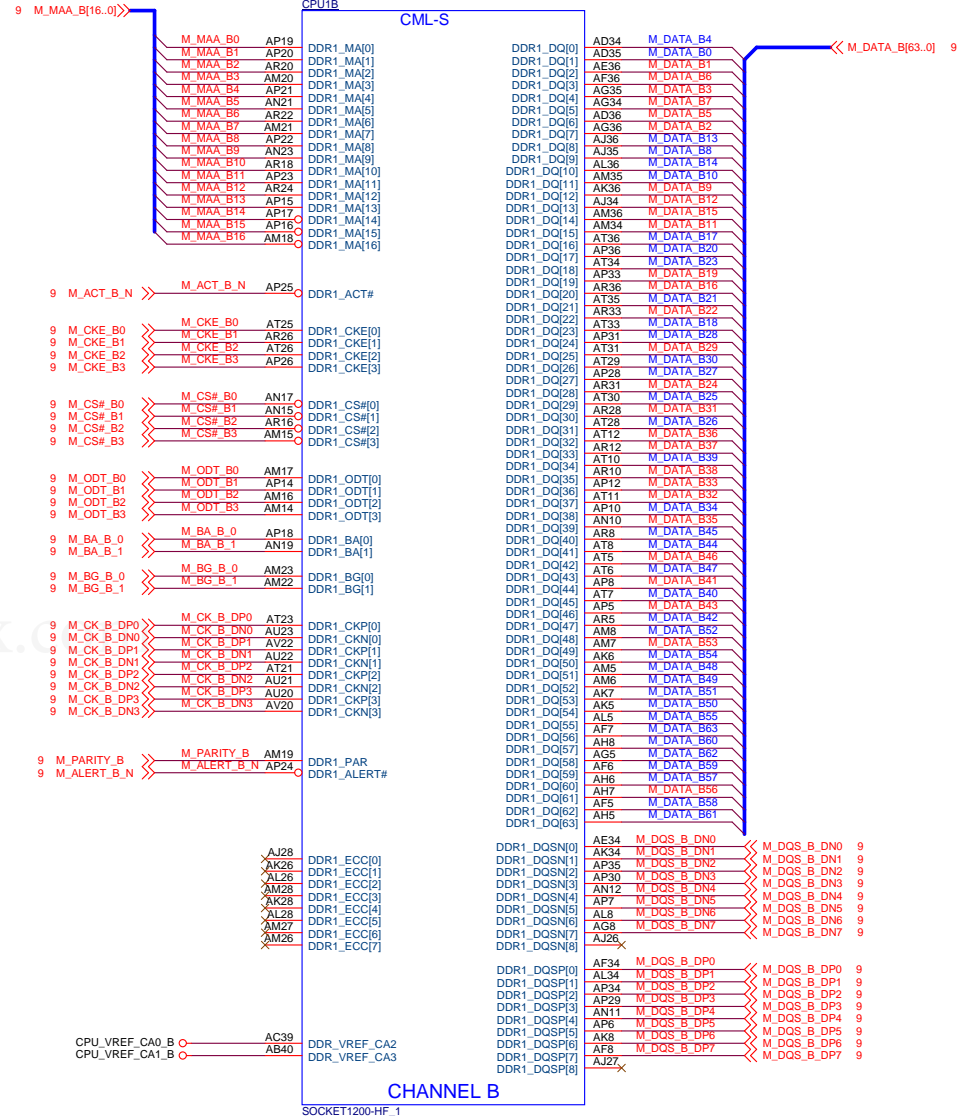
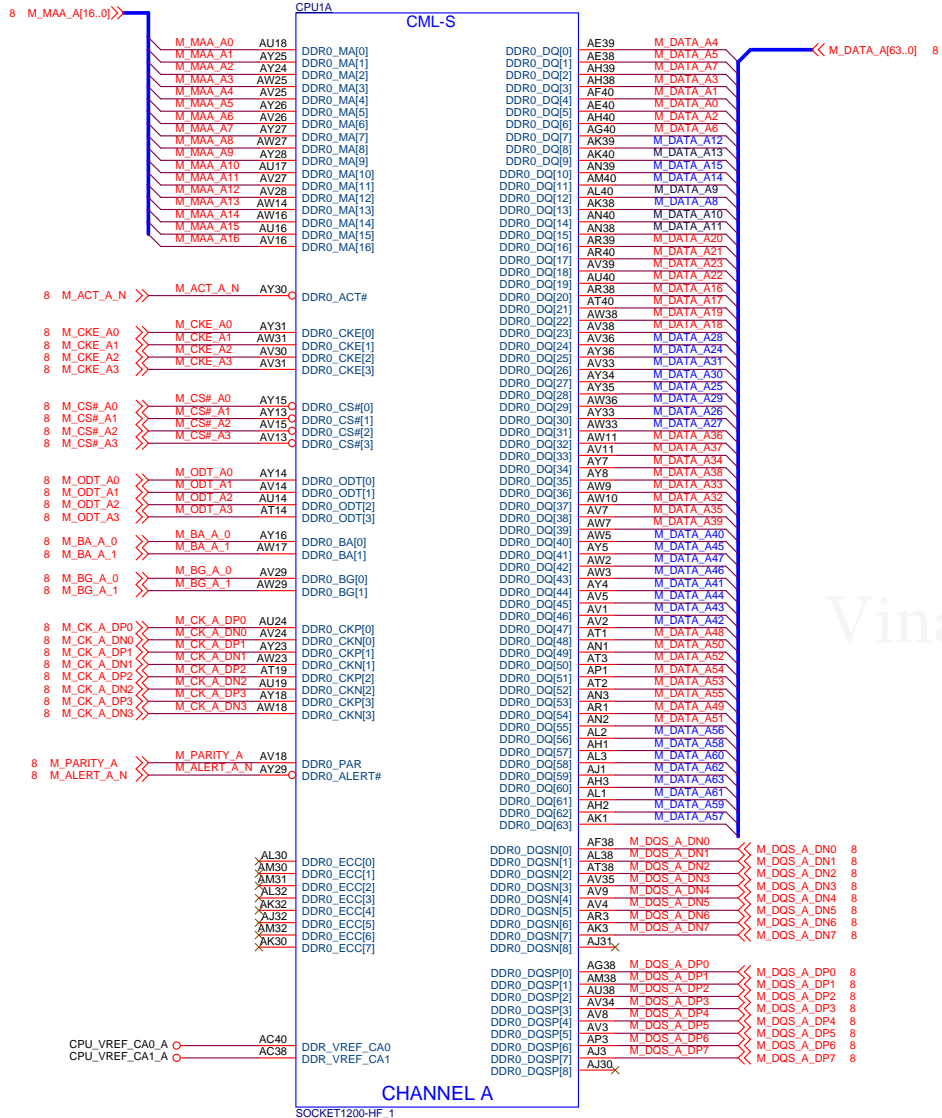
MICRO-STAR INT'L CO.,LTD		
MS-7C75		
Size Custom	Document Description Cover Sheet	Rev 1.1
Date: Thursday, December 05, 2019 Sheet 1 of 70		

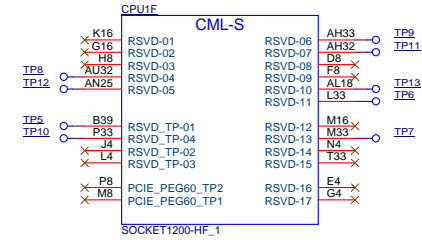
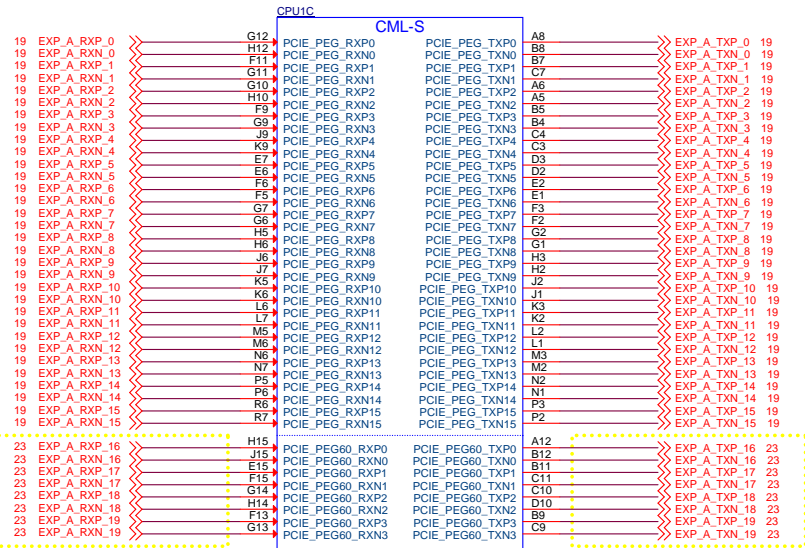
# MS-7C75 Block Diagram



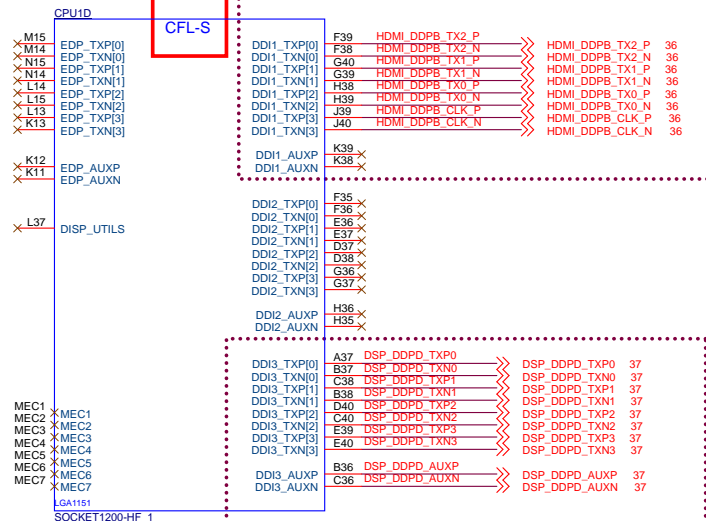
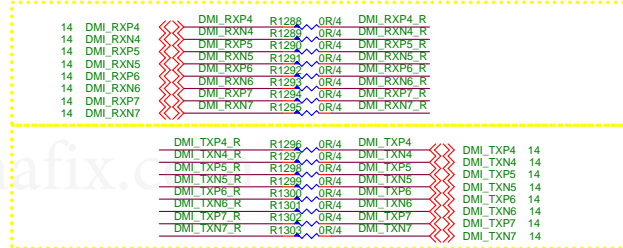


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	<b>MS-7C75</b>		
	Size Custom	Document Description <b>CPU-Control/MISC/CFG</b>	Rev 1.1
	Date: Thursday, December 05, 2019		Sheet 3 of 70





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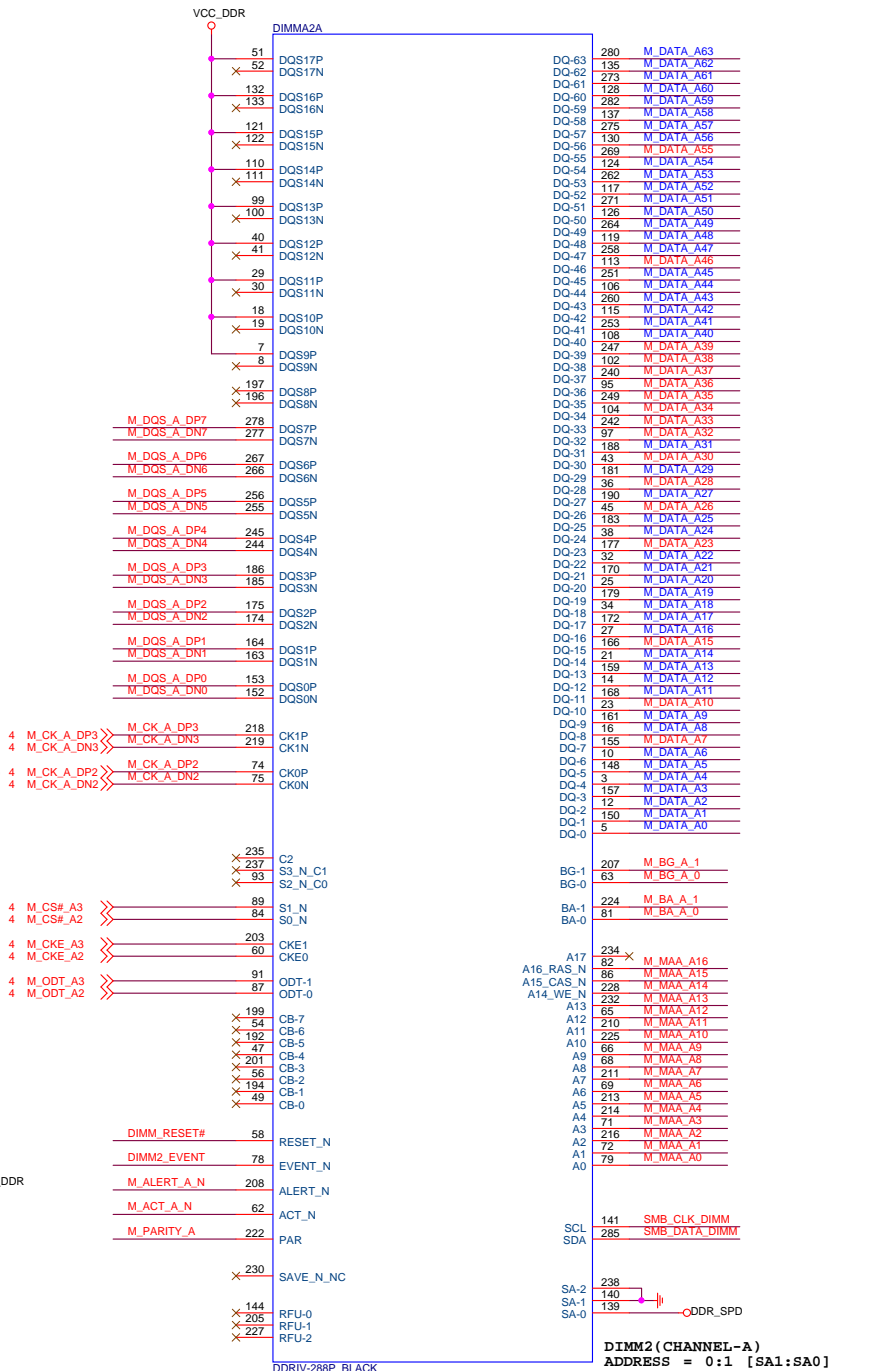
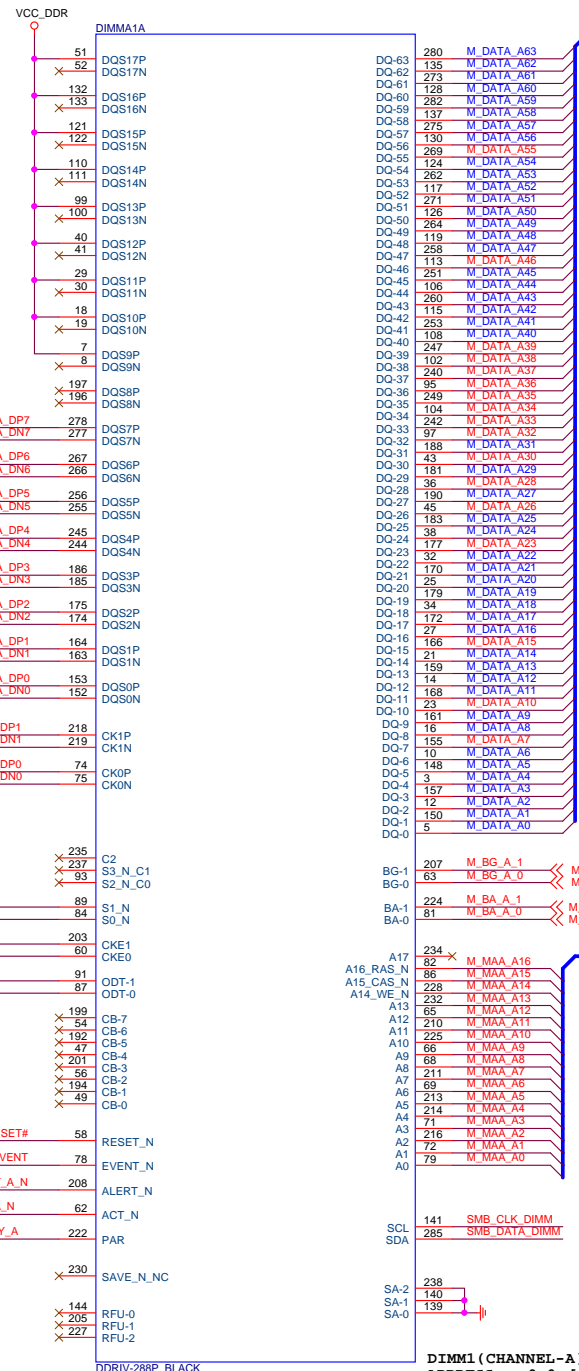
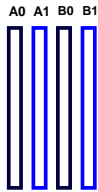
MS-7C75

Size Custom Document Description CPU-PEG/Display/RSB Rev 1.1 Date: Thursday, December 05, 2019 Sheet 5 of 70



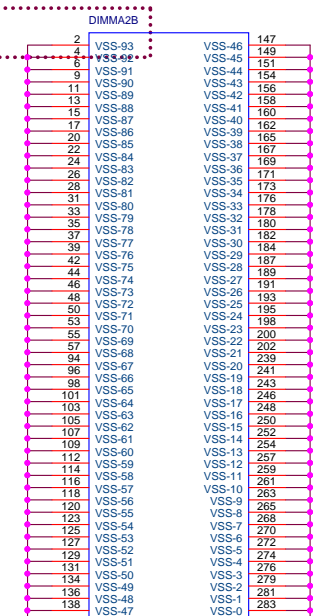
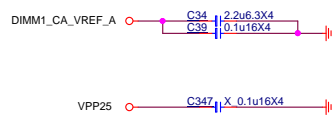
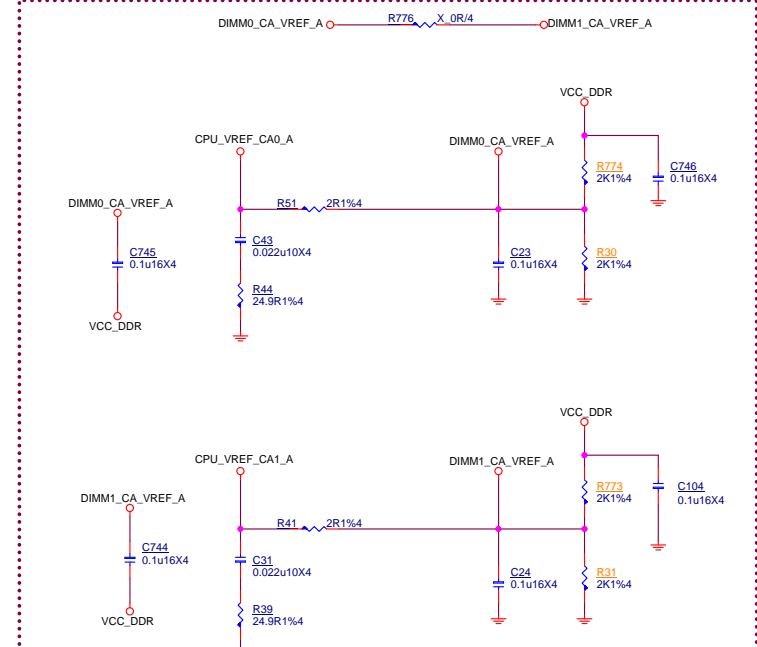
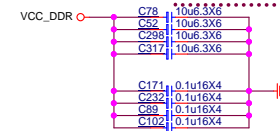
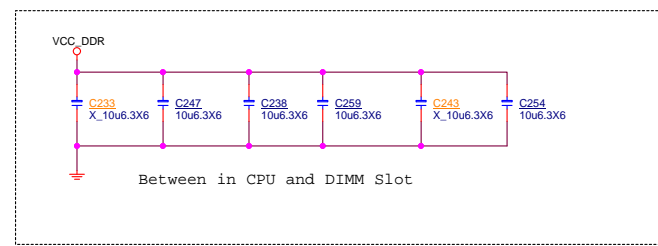




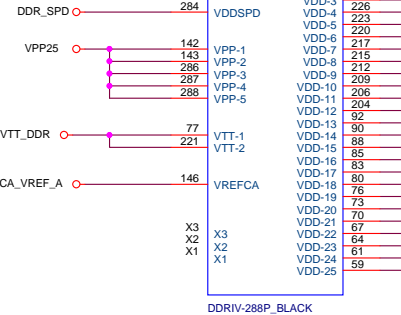




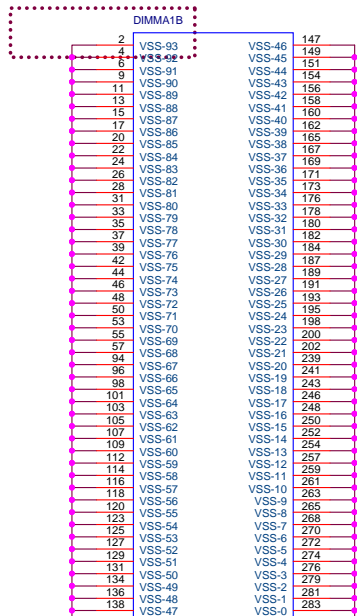
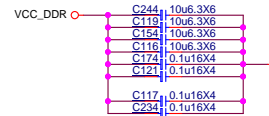
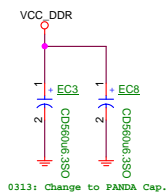




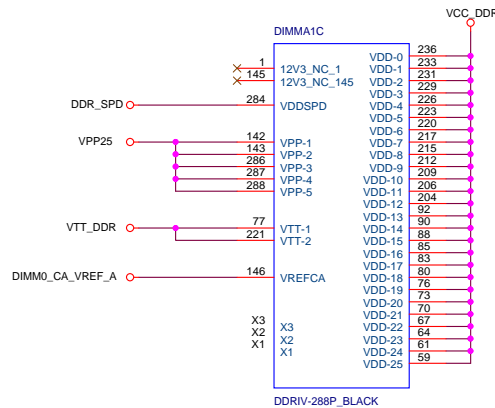
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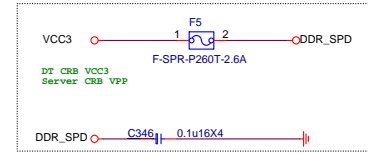
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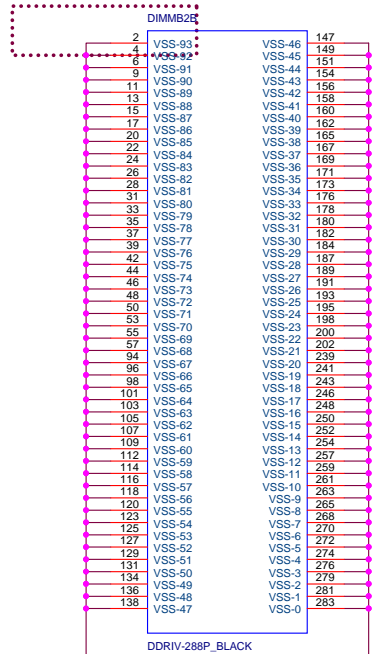
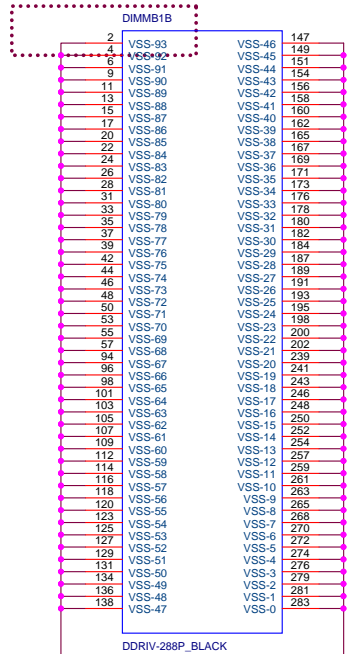
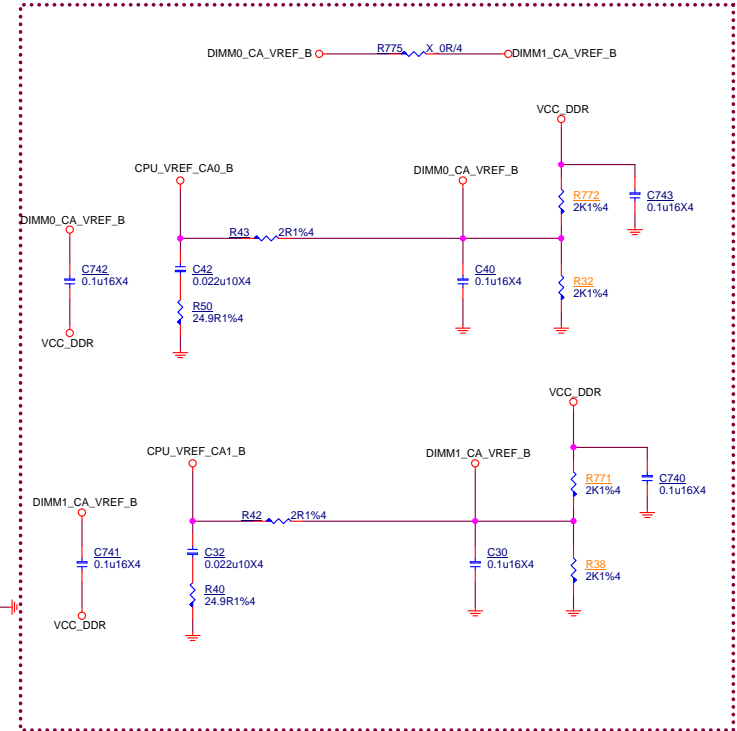
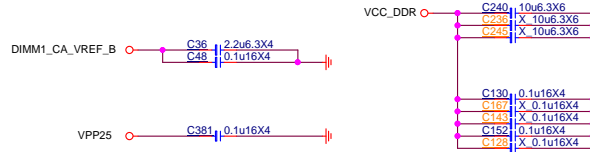
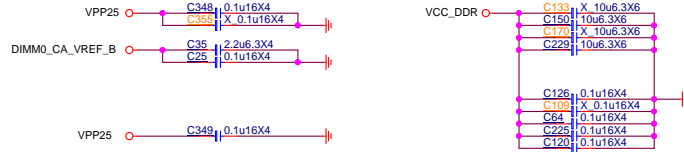
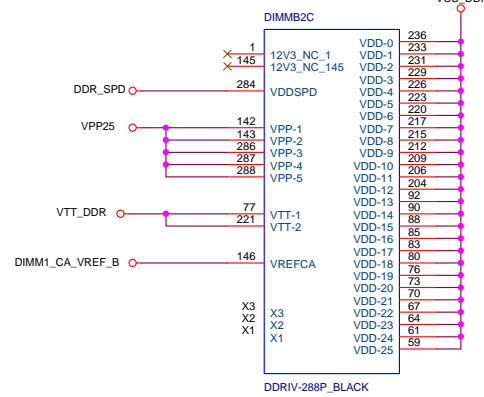
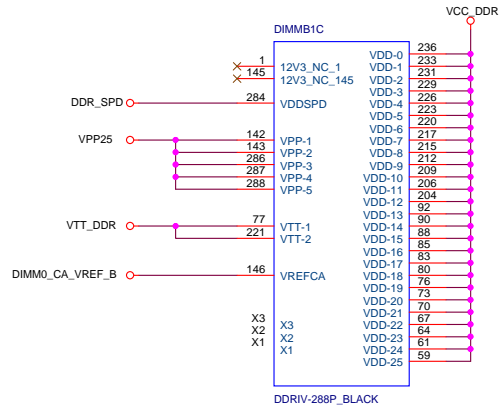


DDRIV-288P\_BLACK



DDRIV-288P\_BLACK

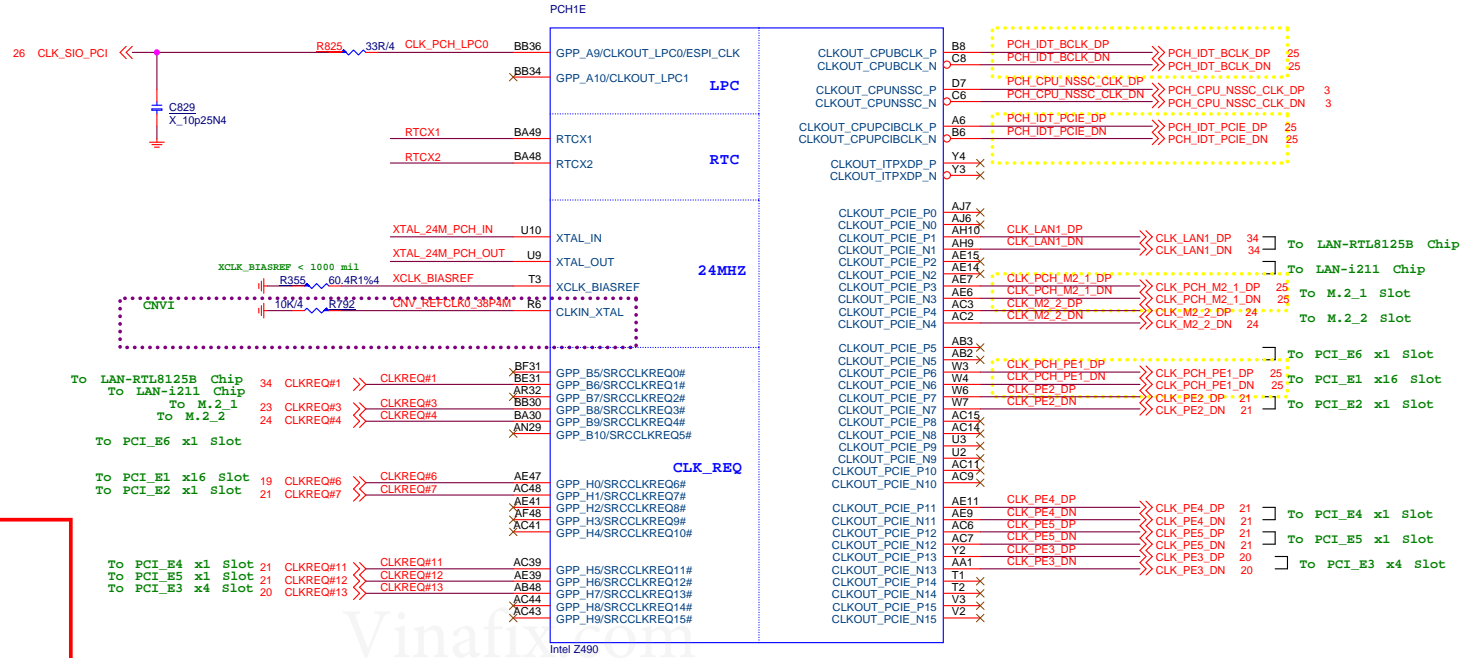
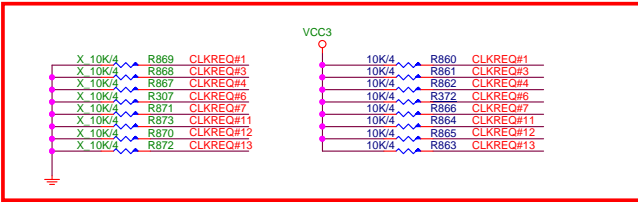
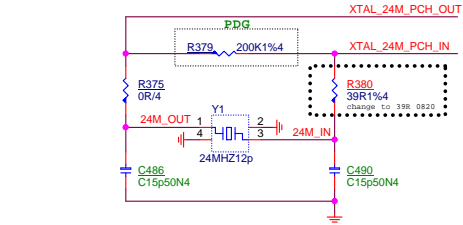
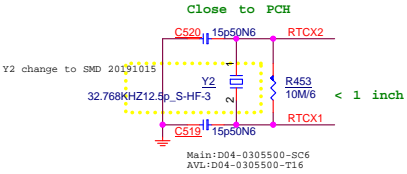




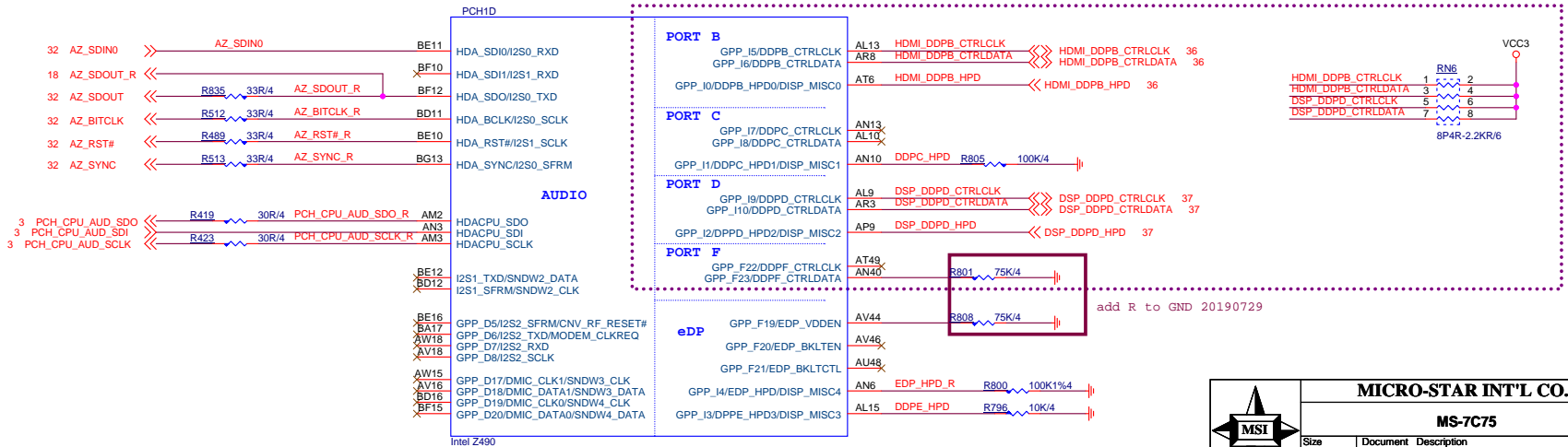
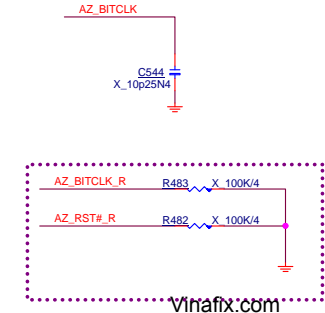


# PCH\_CLK

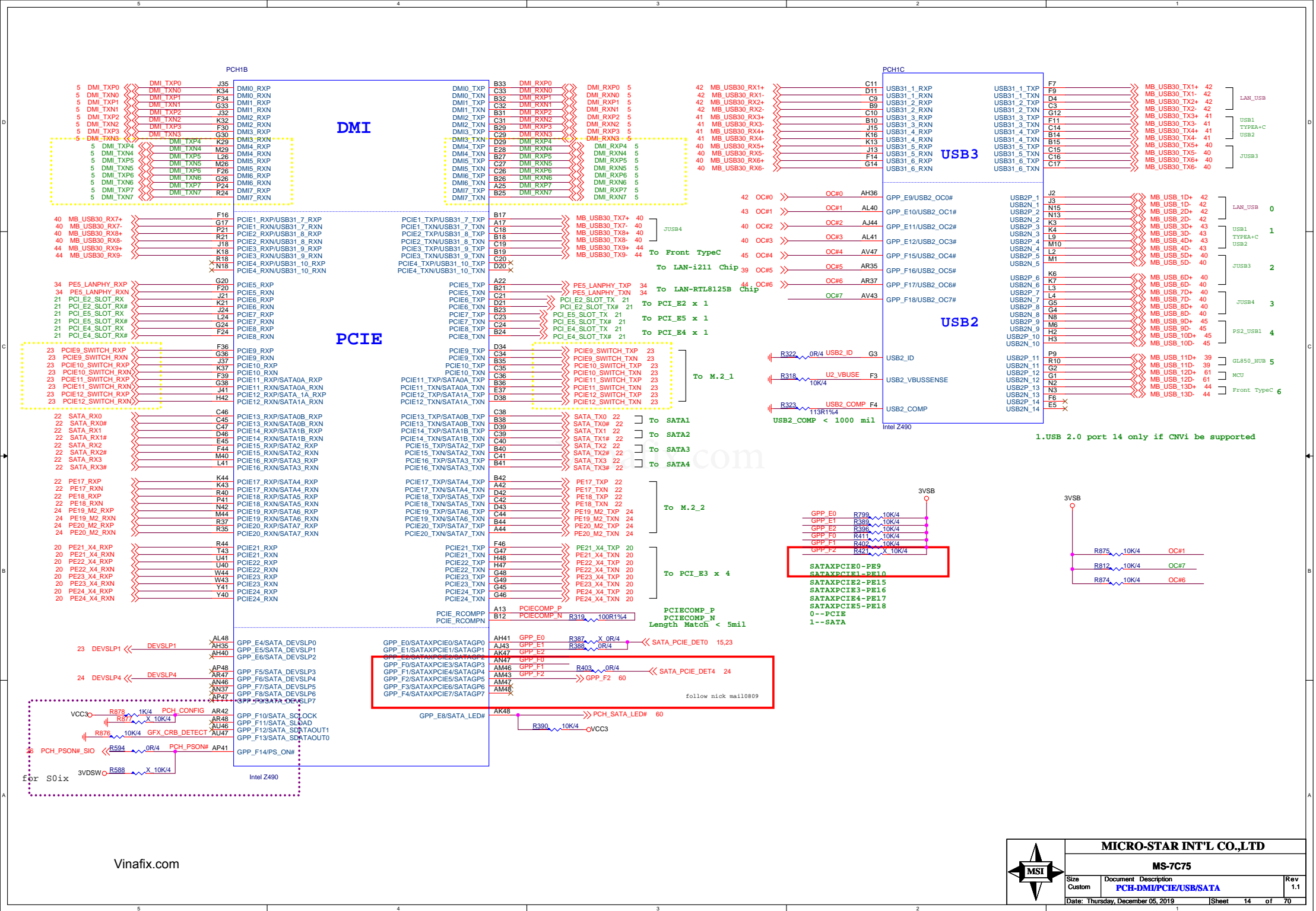
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# PCH\_AUDIO











BASE:7.169A  
DMI:1.116A  
VCCPRIM\_1P05  
PCI1 GEN3:0.178A\*15=2.67A  
PCI2 GEN2:0.152A\*1=0.152A  
USB3\_2 GEN2:0.221A\*2=0.442A  
USB3\_2 GEN1:0.155A\*7=1.085A  
SATA:0.167A\*6=1.002A  
Total:13.616A

13.616+0.106+0.421+0.145+0.005+0.219=14.512A

PCH1G

AA22 VCCPRIM\_1P05\_0  
AA23 VCCPRIM\_1P05\_1  
AB20 VCCPRIM\_1P05\_2  
AB22 VCCPRIM\_1P05\_3  
AB23 VCCPRIM\_1P05\_4  
AB27 VCCPRIM\_1P05\_5  
AB28 VCCPRIM\_1P05\_6  
AB30 VCCPRIM\_1P05\_7  
AD20 VCCPRIM\_1P05\_8  
AD23 VCCPRIM\_1P05\_9  
AD27 VCCPRIM\_1P05\_10  
AD28 VCCPRIM\_1P05\_11  
AD30 VCCPRIM\_1P05\_12  
AD31 VCCPRIM\_1P05\_13  
AE17 VCCPRIM\_1P05\_14  
AF23 VCCPRIM\_1P05\_15  
AF27 VCCPRIM\_1P05\_16  
AF30 VCCPRIM\_1P05\_17  
AF31 VCCPRIM\_1P05\_18  
AG31 VCCPRIM\_1P05\_19  
D1 VCCPRIM\_1P05\_20  
E1 VCCPRIM\_1P05\_21  
U26 VCCPRIM\_1P05\_22  
U29 VCCPRIM\_1P05\_23  
V25 VCCPRIM\_1P05\_24  
V27 VCCPRIM\_1P05\_25  
V28 VCCPRIM\_1P05\_26  
V30 VCCPRIM\_1P05\_27  
V31 VCCPRIM\_1P05\_28

W31 VCCPRIM\_MPHY\_1P05  
W22 VCCDUSB\_1P05\_1  
W23 VCCDUSB\_1P05\_2  
C49 VCCAMPHYPLL\_1P05\_1  
D49 VCCAMPHYPLL\_1P05\_2  
E49 VCCAMPHYPLL\_1P05\_3

P2 VCCA\_XTAL\_1P05\_1  
P3 VCCA\_XTAL\_1P05\_2

W19 VCCA\_SRC\_1P05\_1  
W20 VCCA\_SRC\_1P05\_2

C1 VCCAPLL\_1P05\_4  
C2 VCCAPLL\_1P05\_5

A19 VCCA\_BCLK\_1P05

B1 VCCAPLL\_1P05\_1  
B2 VCCAPLL\_1P05\_2  
B3 VCCAPLL\_1P05\_3

K47 VCCMPHY\_SENSE  
K46 VSSMPHY\_SENSE

BG45 VCCDSW\_1P05\_1  
BG46 VCCDSW\_1P05\_2

C529 1u6.3X4

Intel Z490

## POWER

VCCPRIM\_3P3\_0  
VCCPRIM\_3P3\_1  
VCCPRIM\_3P3\_2  
VCCPRIM\_3P3\_3  
VCCPRIM\_3P3\_4

VCCSPI

VCCRTC\_1  
VCCRTC\_2

VCCDSW\_3P3\_1  
VCCDSW\_3P3\_2

VCCCHDA

VCCPRIM\_1P8\_3  
VCCPRIM\_1P8\_4  
VCCPRIM\_1P8\_5  
VCCPRIM\_1P8\_6  
VCCPRIM\_1P8\_7

VCCPHVLD0\_1P8\_1  
VCCPHVLD0\_1P8\_2

VCCDPHY\_1P24\_4  
VCCDPHY\_1P24\_5

VCCDPHY\_1P24\_1  
VCCDPHY\_1P24\_2  
VCCDPHY\_1P24\_3

VCCPGPPA

VCCPGPPBC\_1  
VCCPGPPBC\_2

VCCPGPPD

VCCPGPPEF\_1  
VCCPGPPEF\_2

VCCPGPPHK\_1  
VCCPGPPHK\_2

VCCPGPPG\_3P3

DCPRTC\_1  
DCPRTC\_2

AN9 0.383A 3VSB  
V23 0.383+0.008+0.344+0.175+0.263+0.145=1.318A  
AY8  
BB7  
AT44

AN44 0.03A VSB\_SPI

BC49 0.6mA VBAT\_PCH  
BD49

BE49 0.113A 3VDSW  
BE49

BB14 0.008A 3VSB

AG19 0.183A 3VSB External LDO  
AG20 0.183+0.03+0.061+0.084+0.358A  
AN15  
AR15  
BB11

AF19 PCH\_1P8\_LDO  
AF20

AK22 PCH\_1P24\_VSB\_LDO  
AK23

AJ22 LDO output  
AJ23 PCH\_1P24\_VSB  
BG5

AN32 0.061A VCCPGPPA

AN26 0.111A 3VSB  
AP26 C818 0.1u16X4

AN24 0.084A VCCPGPPD

AE35 0.175A 3VSB  
AE36 C820 0.1u16X4

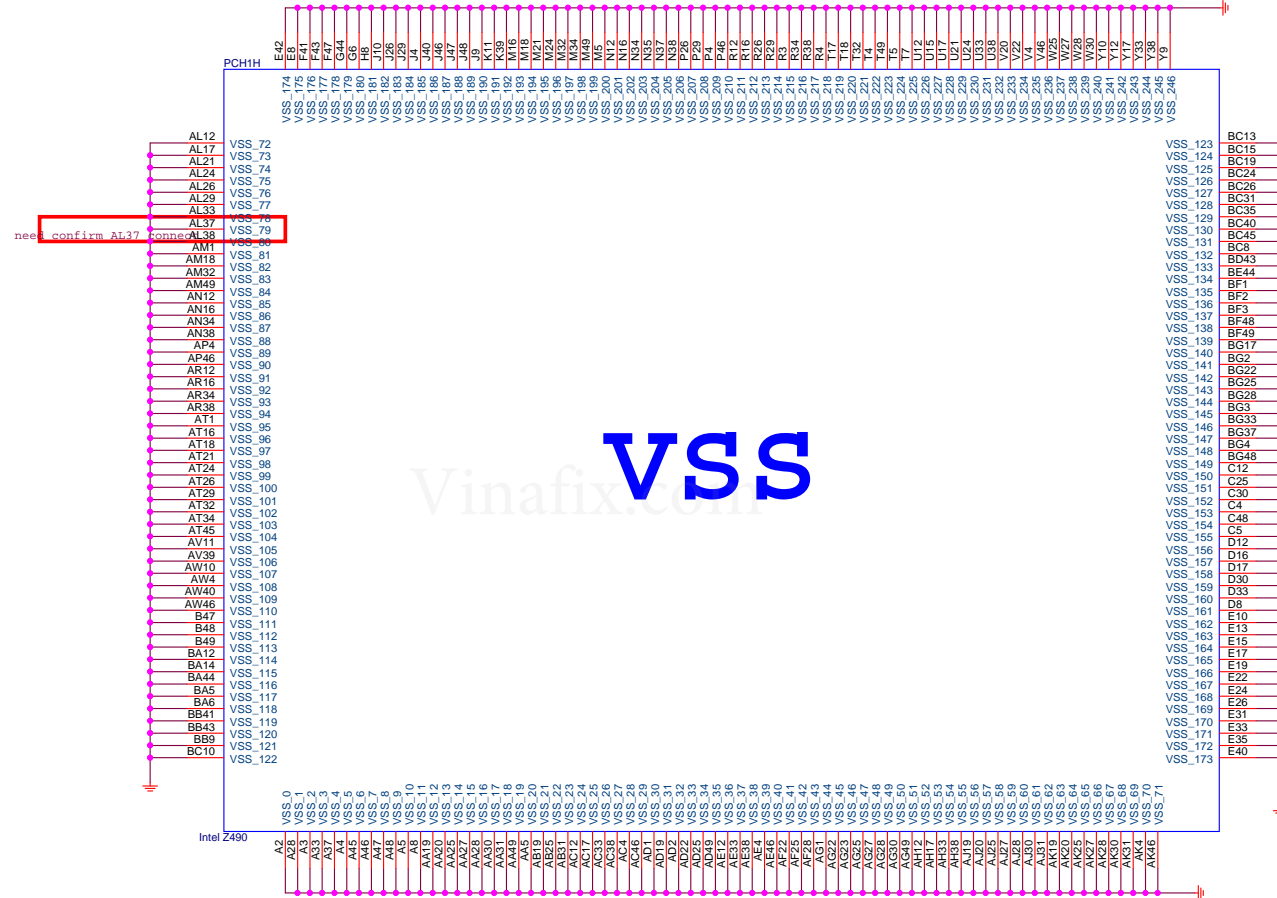
AC35 0.263A 3VSB  
AC36 C807 0.1u16X4

AN21 0.145A

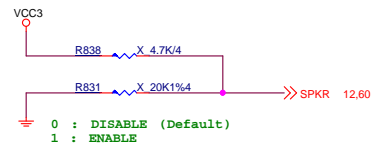
BF47 0.03A DCPRTC  
BG47

C524 0.1u16X4

C821 0.1u16X4  
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C824 0.1u16X4  
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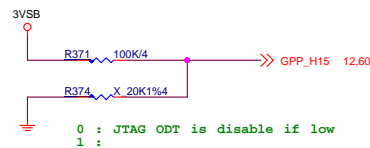


## TOP Swap



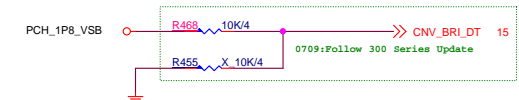
Internal Pull-down is disabled after PCH\_PWROK is high.

## ODT Disable



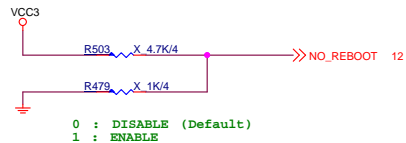
Internal Pull-down is disabled after RSMRST# de-assert.

## XTAL FREQUENCY SELECTION



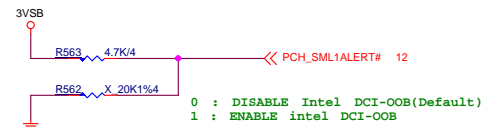
This Signal has a Weak Internal Pull-down.  
An External Pull-up is Required On this Strap Since 38.4 MHz XTAL is Not Supported On the PCH.  
0 = 38.4 XTAL Frequency Selected. (Default)  
1 = 24MHz XTAL Frequency Selected.

## No Reboot



Internal Pull-down is disabled after PCH\_PWROK is high.

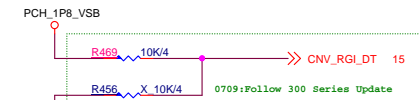
## DCI Enable



Internal Pull-down is disabled after RSMRST# de-assert.

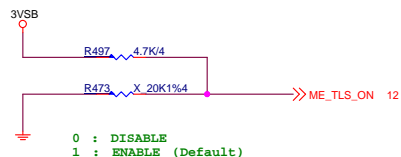
## Modem Reference Clock Source Select

Note: When a RF Companion Chip is Connected to The PCH CNVi Interface, The Device Internal Pull Down Resistor will Pull the Strap Load to Enable CNVi Interface.



A Weak External Pull-up is Required.  
0 = Integrated CNVi Enable.  
1 = Integrated CNVi Disable.

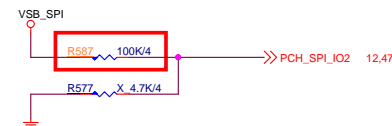
## TLS confidentiality



Internal Pull-down is disabled after RSMRST# de-assert.

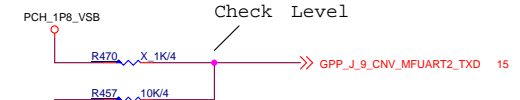
## Reserved

stuff 100K if pull up to 3.3V  
stuff 75K if pull up to 1.8V



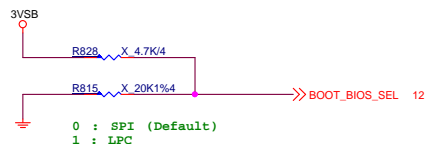
## 1.8V VCCPSPI

need check level  
Check Level



SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE  
0 = VCCPSPI IS CONNECTED TO 3.3V RAIL - DEFAULT  
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL  
PCH HAS INTERNAL 20K PD

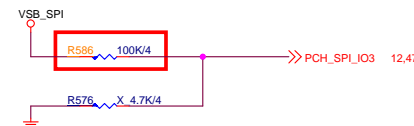
## Boot BIOS



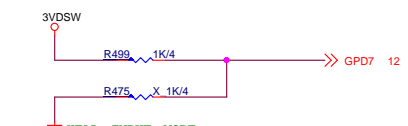
Internal Pull-down is disabled after PCH\_PWROK is high.

## Reserved

stuff 100K if pull up to 3.3V  
stuff 75K if pull up to 1.8V

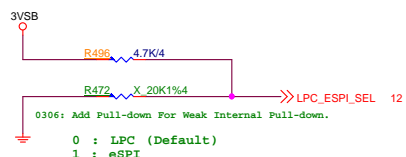


## Reserved



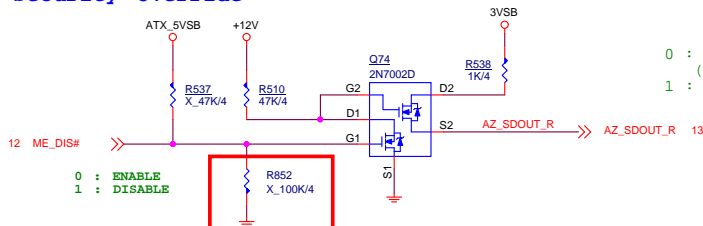
XTAL INPUT MODE  
0 = XTAL INPUT IS SINGLE-ENDED  
1 = XTAL INPUT IS DIFFERENTIAL  
PCH HAS INTERNAL 20K PD

## LPC eSPI Mode



Internal Pull-down is disabled after RSMRST# de-assert.

## Flash Descriptor Security Override

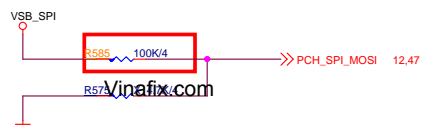


0 : Enable security measures defined in the Flash Descriptor. (Default)  
1 : DISABLE:Flash Descriptor Security(Override).

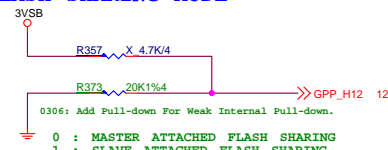
Internal Pull-down is disabled after PCH\_PWROK is high.

## Reserved

stuff 100K if pull up to 3.3V  
stuff 75K if pull up to 1.8V



## eSPI FLASH SHARING MODE



Internal Pull-down is disabled after RSMRST# de-assert.



MICRO-STAR INT'L CO.,LTD

MS-7C75

Size Custom

Document Description

PCH-Strap

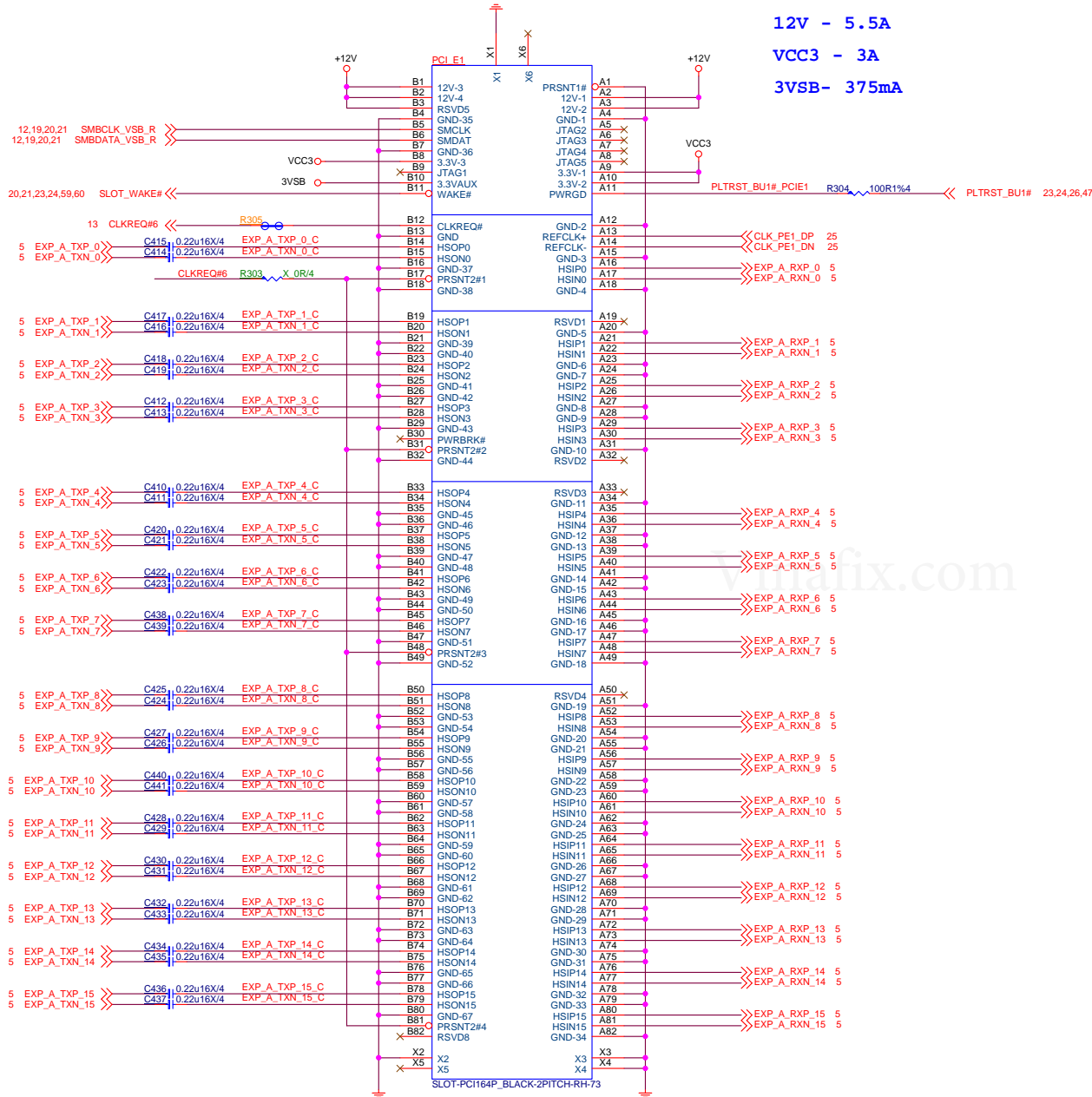
Rev 1.1

Date: Friday, December 27, 2019

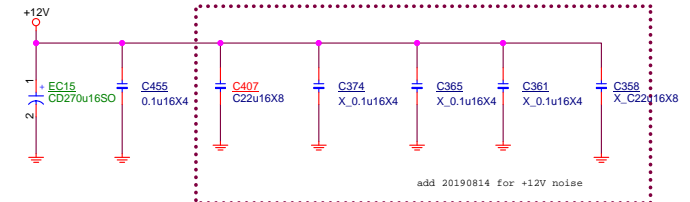
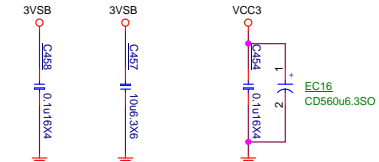
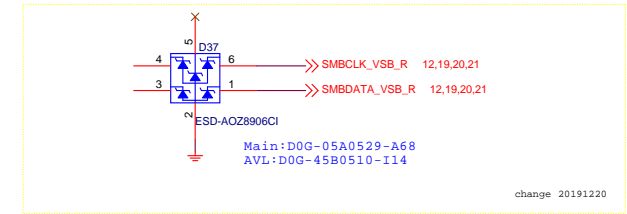
Sheet 18 of 70

# PCI\_Express X16 Slot

12V - 5.5A  
VCC3 - 3A  
3VSB- 375mA

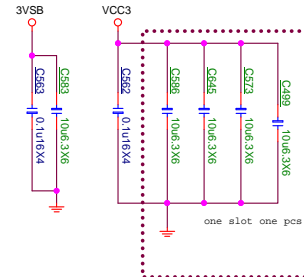
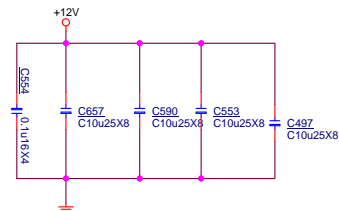
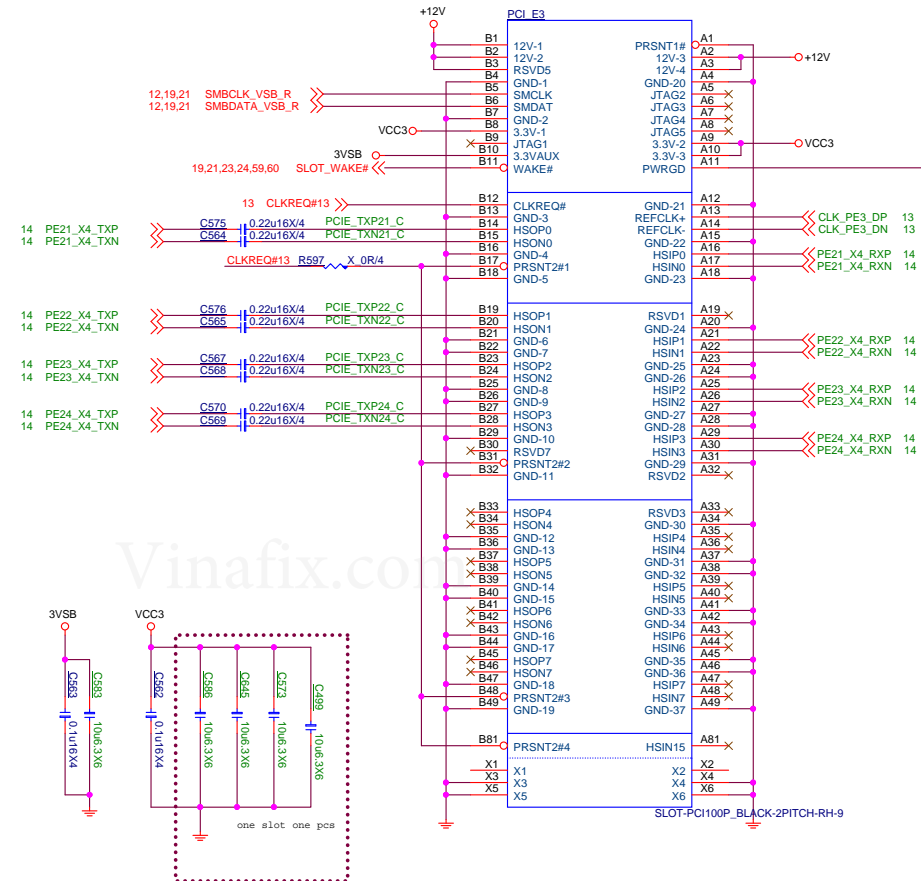


## SMBus ESD



### PCI\_Express X4 Slot

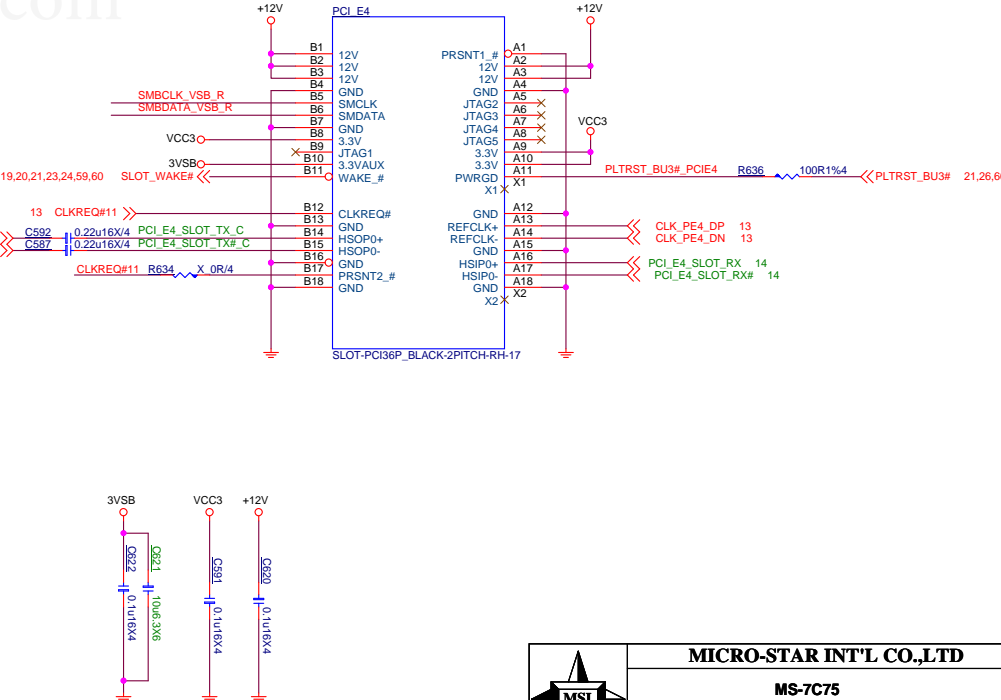
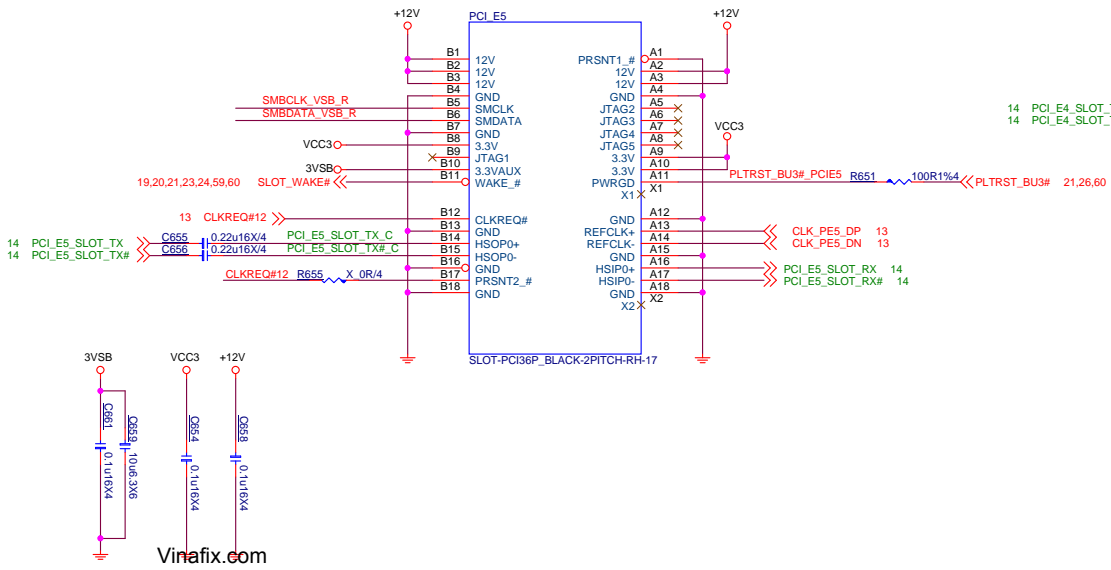
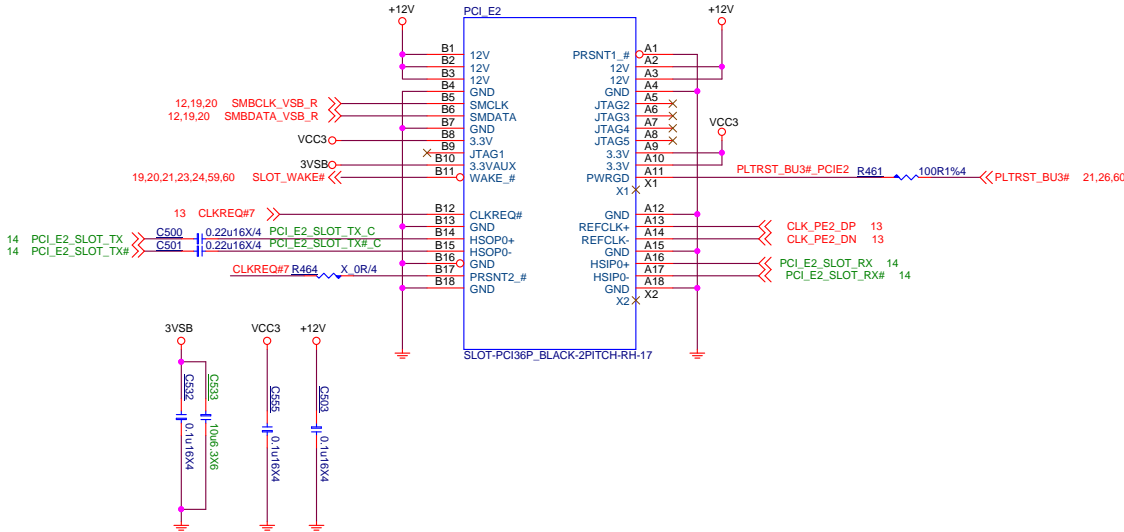
2.1A at +12V  
3A at VCC3  
375mA at 3VSB



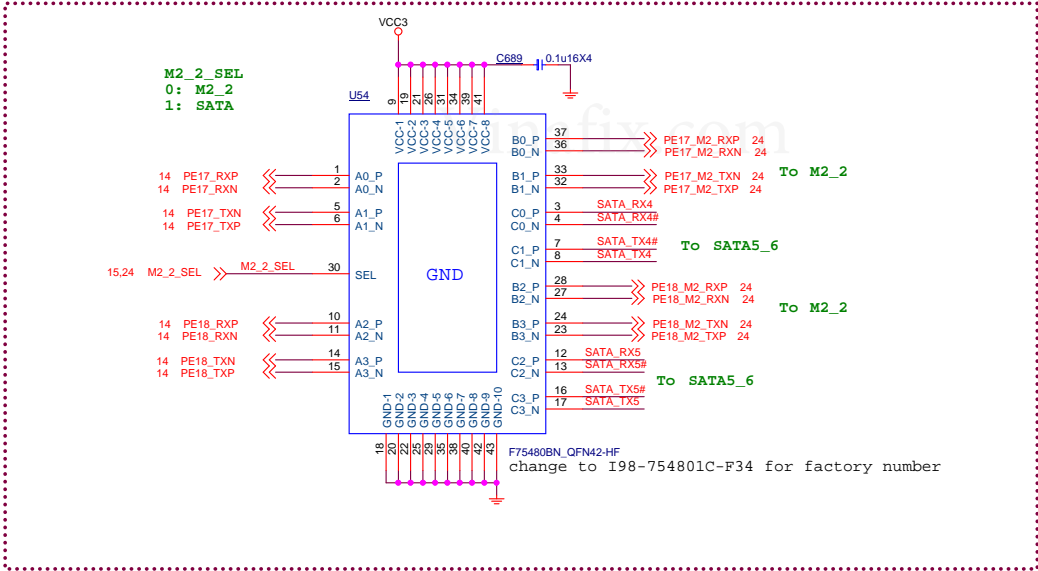
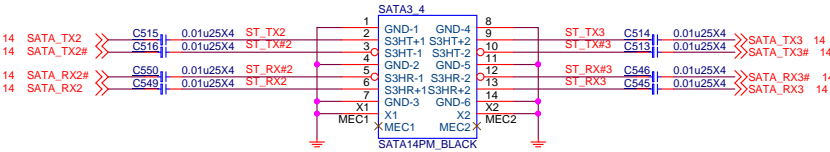
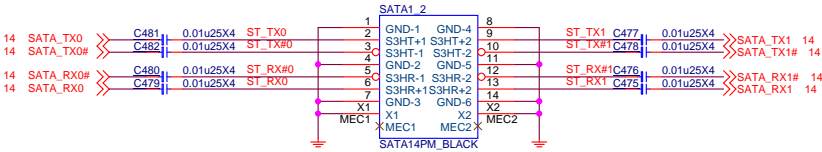


PCH PCIE X1 slot

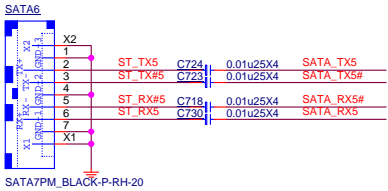
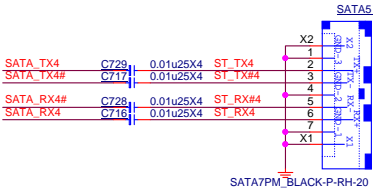
12V - 0.5A  
VCC3 - 3A  
3VSB - 375mA



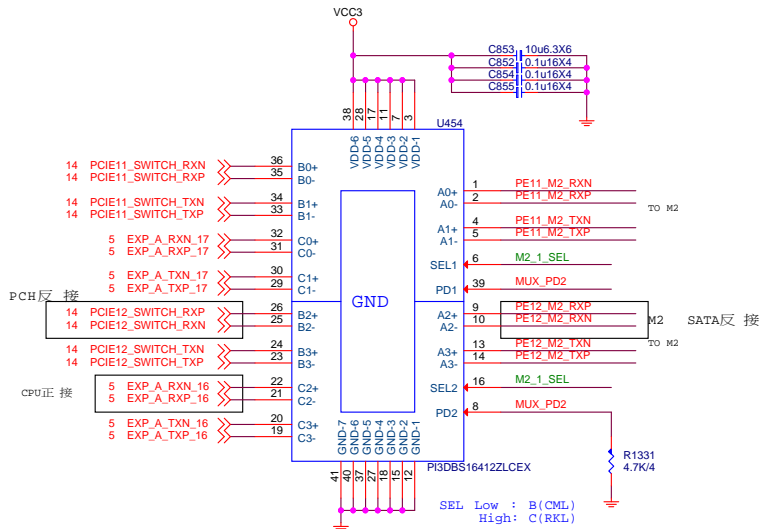
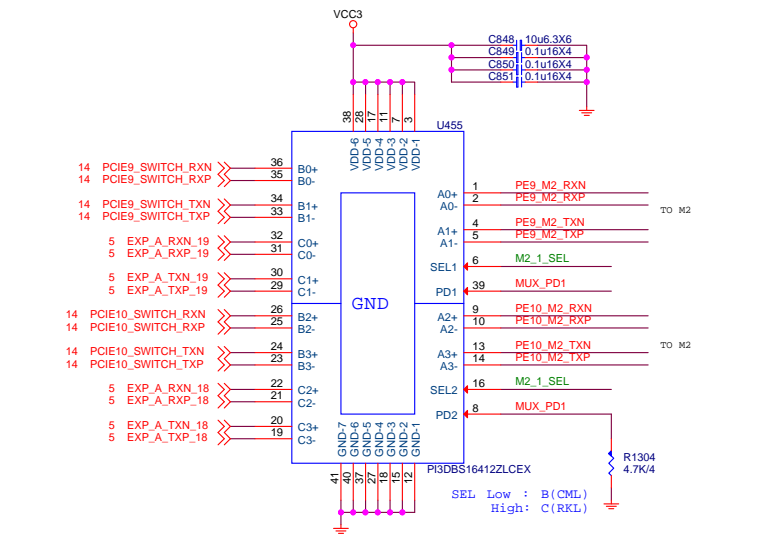
SATA Connector



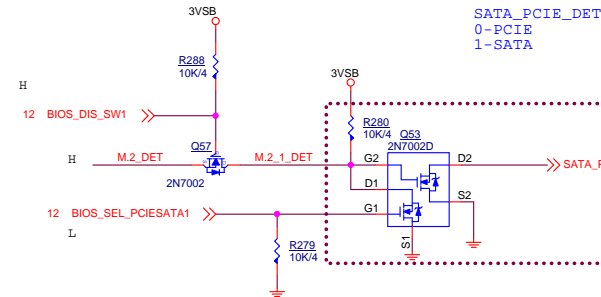
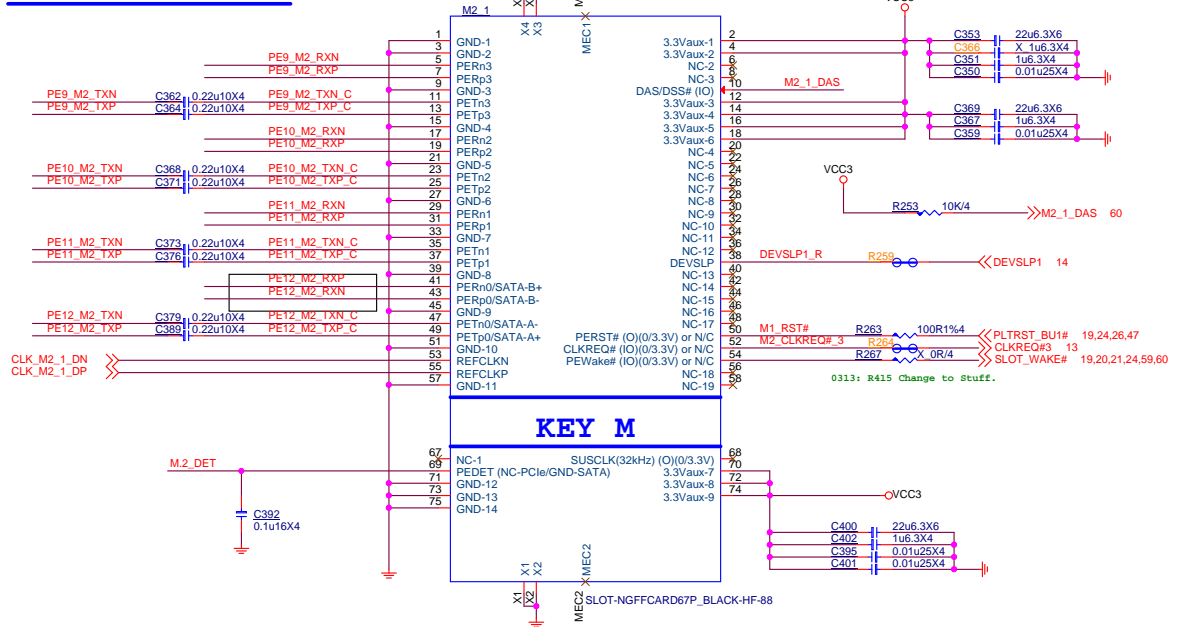
Vinafix.com



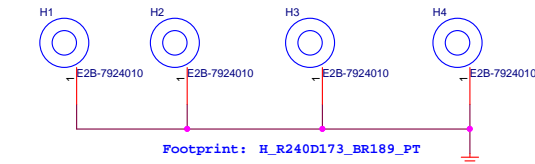
Vinafix.com



## M.2 Connector



## 22 \* 110



## BIOS\_MODE

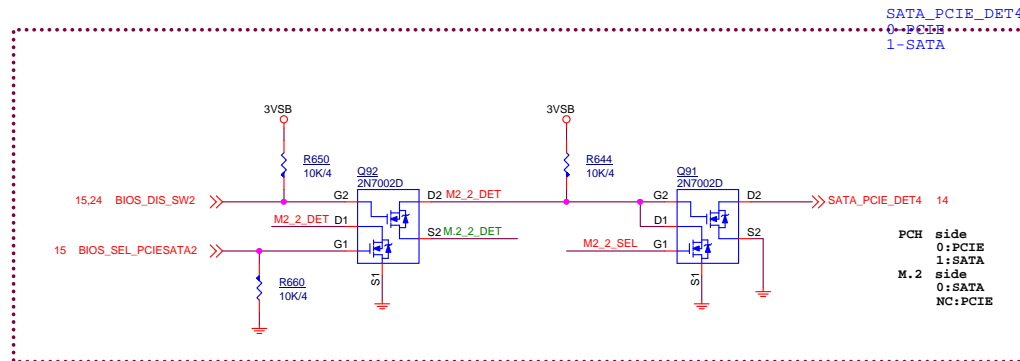
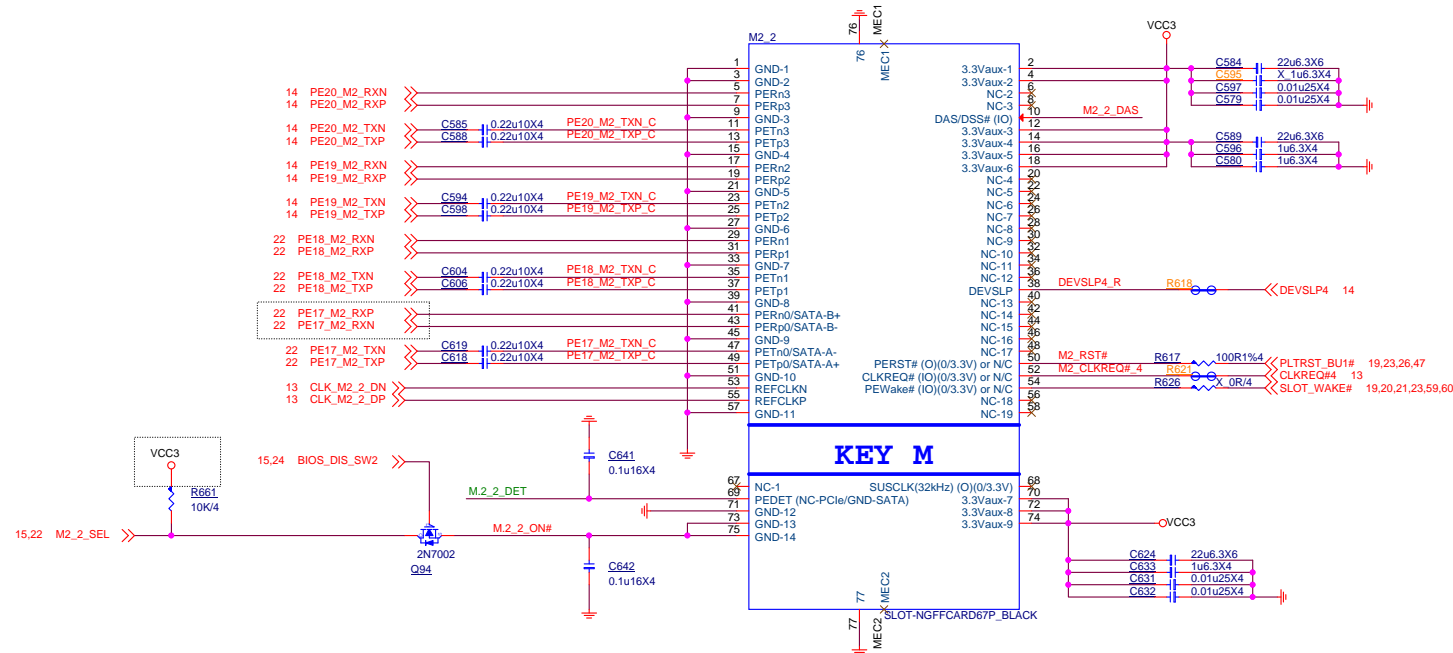
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode	BIOS_CPU_PCH_SEL	
0	1	M2-SATA	GPI (1)	CML (PCH)
0	0	M2-PCIE	GP0 (0)	RKL (CPU)
GPI	GPI	AUTO		



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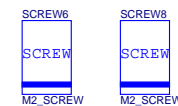
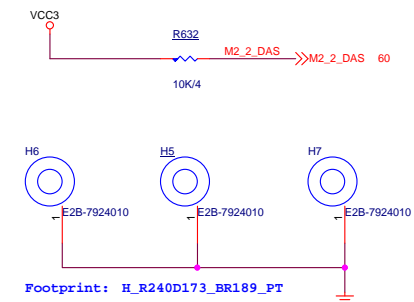


#### BIOS\_MODE

To Switch SATA5\_6

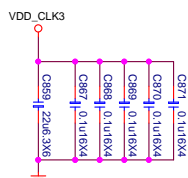
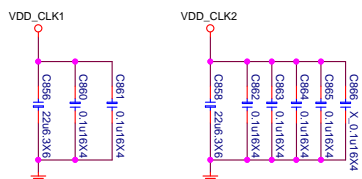
GPP_G7	GPP_G6	GPP_G5		
BIOS_DIS_SW2	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode	SATA_PCIE_DET4
GPI(1)	GPI(1)	GPI(0)	AUTO	
0	1	0	SATA5_6	1
0	0	1	M2-SATA	1
0	0	0	M2-PCIE	0

22 \* 80

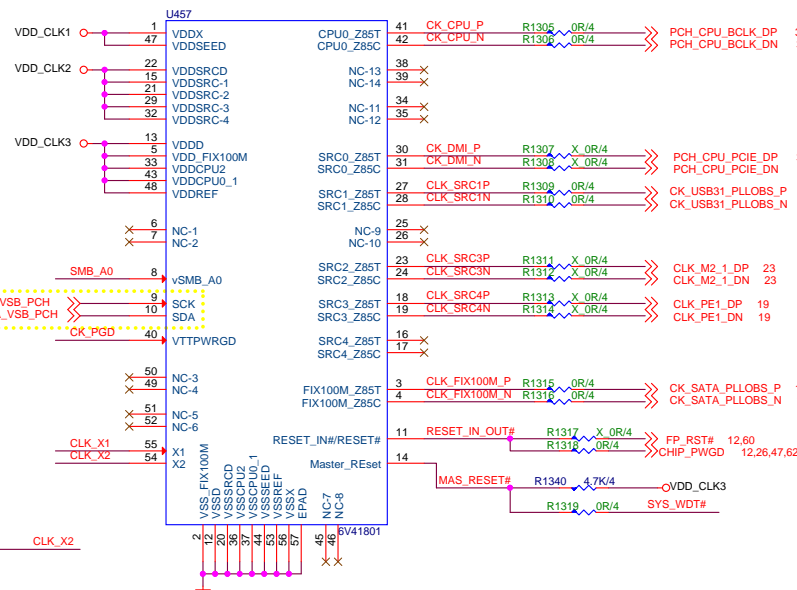


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220mA  
VCC3\_CLK ○ R1328 0R/6 ○ VDD\_CLK1  
VCC3\_CLK ○ R1328 0R/6 ○ VDD\_CLK2  
VCC3\_CLK ○ R1330 0R/6 ○ VDD\_CLK3



SMB_A0	ADDR
0	D2/D3
1	D8/D9



CPU

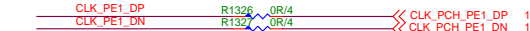
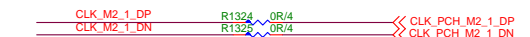
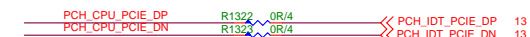
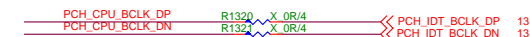
CPU

PCH(USB31)

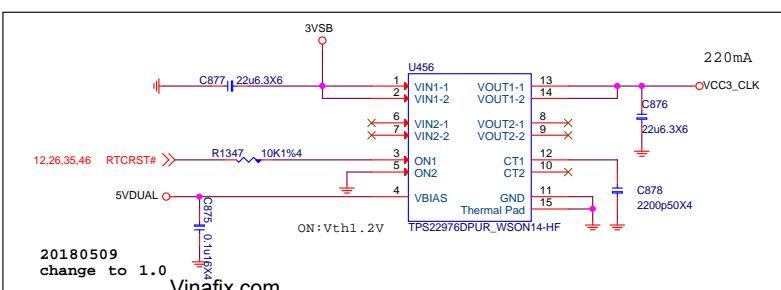
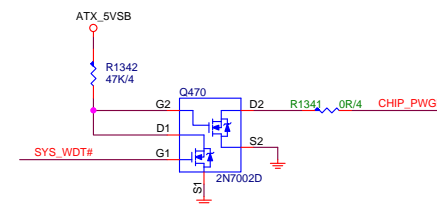
M2\_1

PCI\_E1

PCH(SATA)

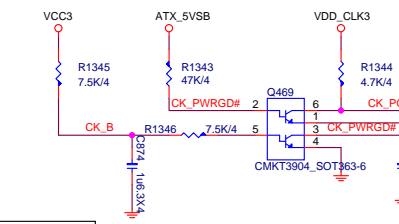
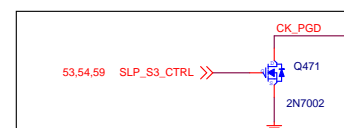


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20180509  
change to 1.0

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MS-7C75			
Size	Document	Description	Rev
Custom		Clock Gen-IDT41801	1.1
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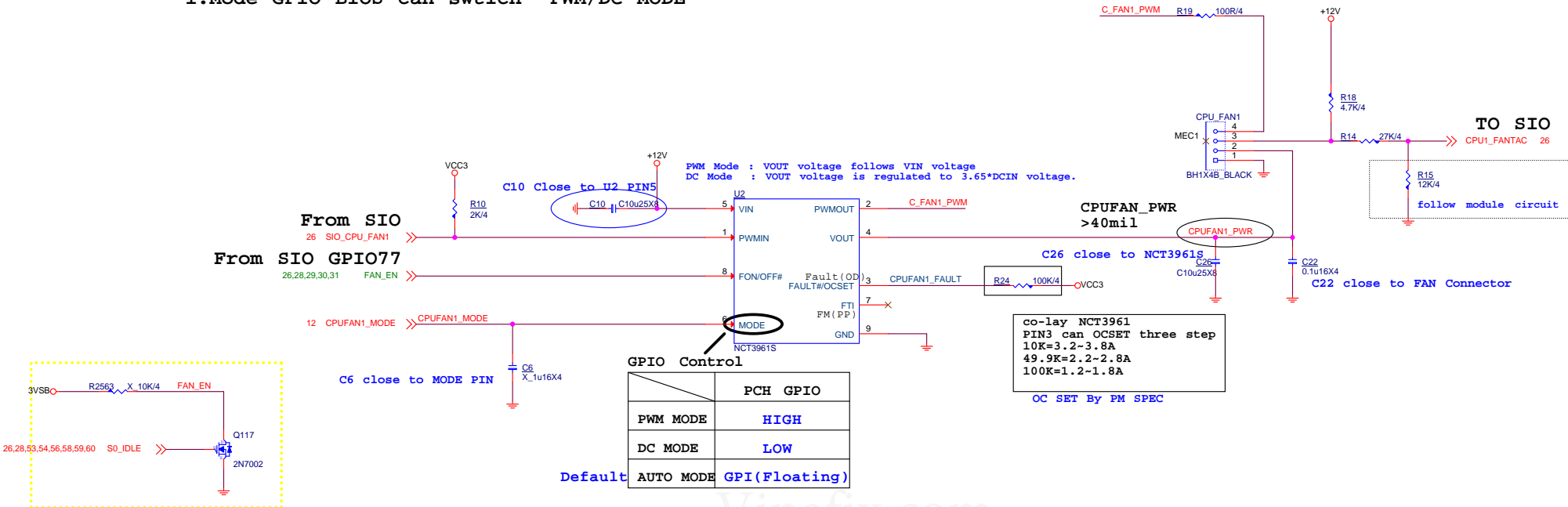






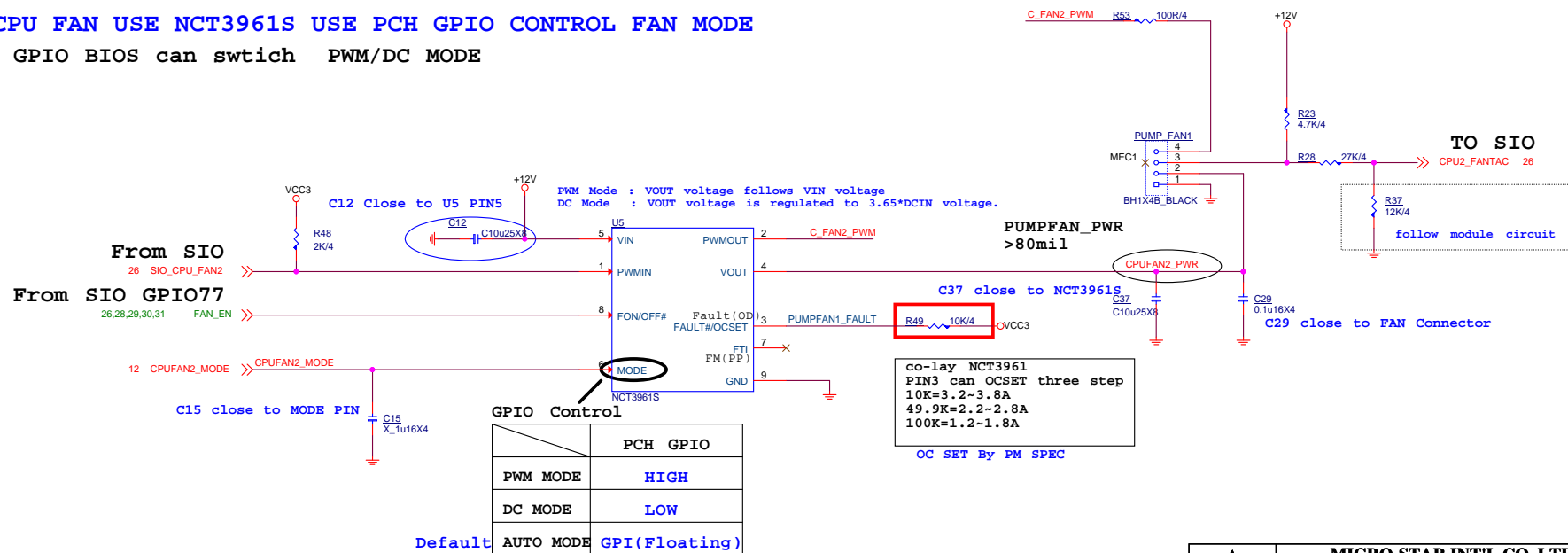
# TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



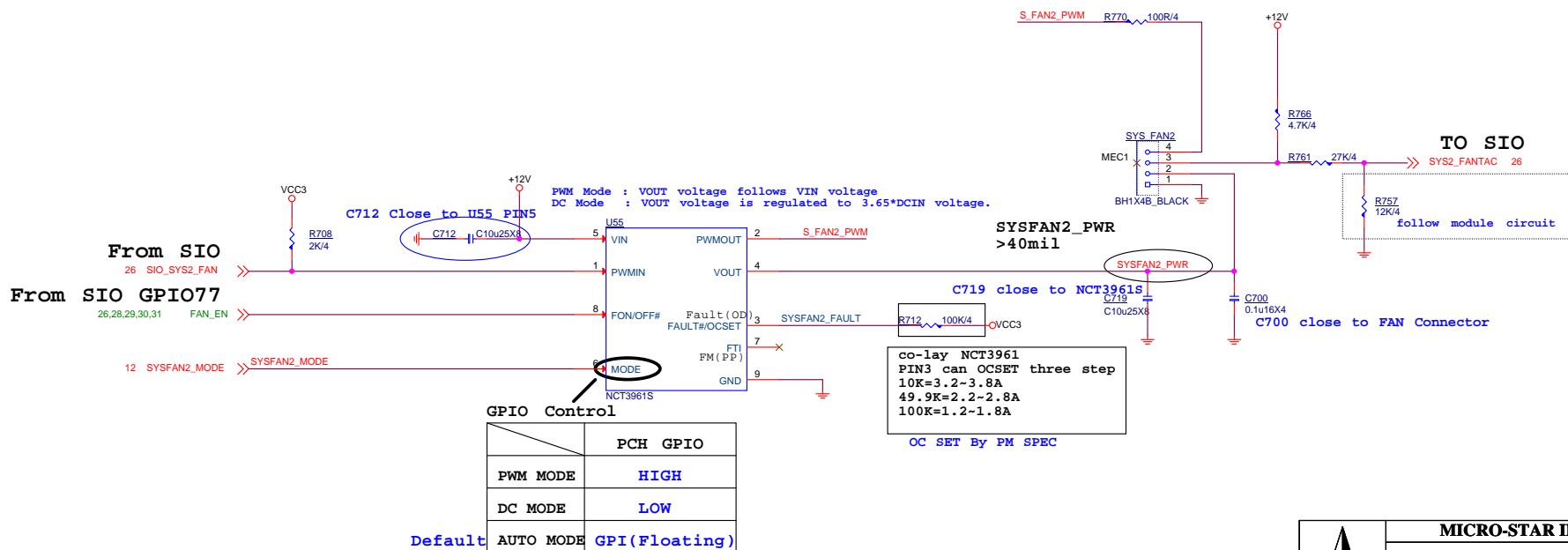
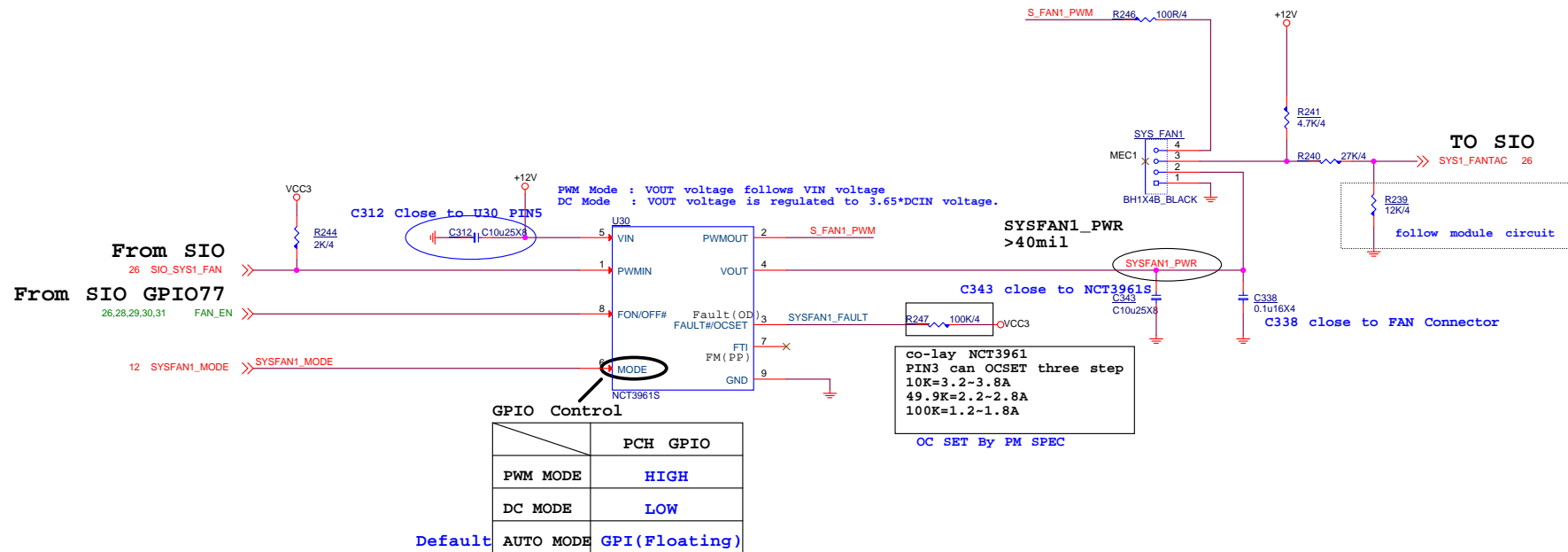
# TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



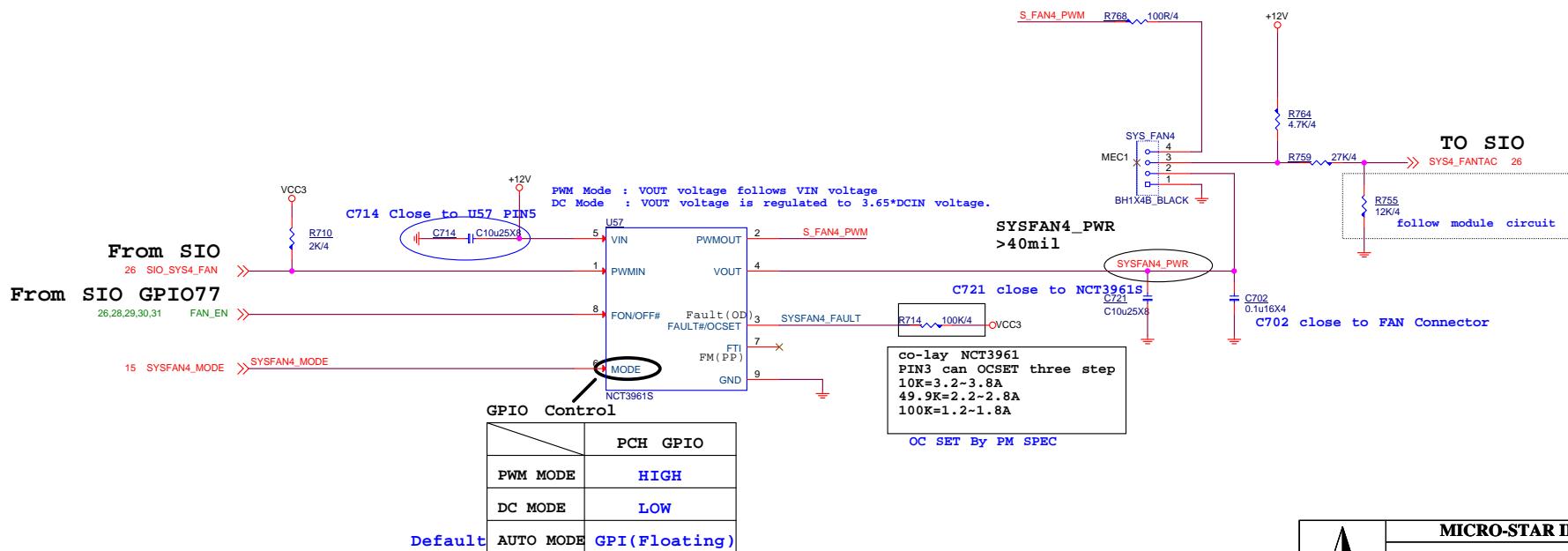
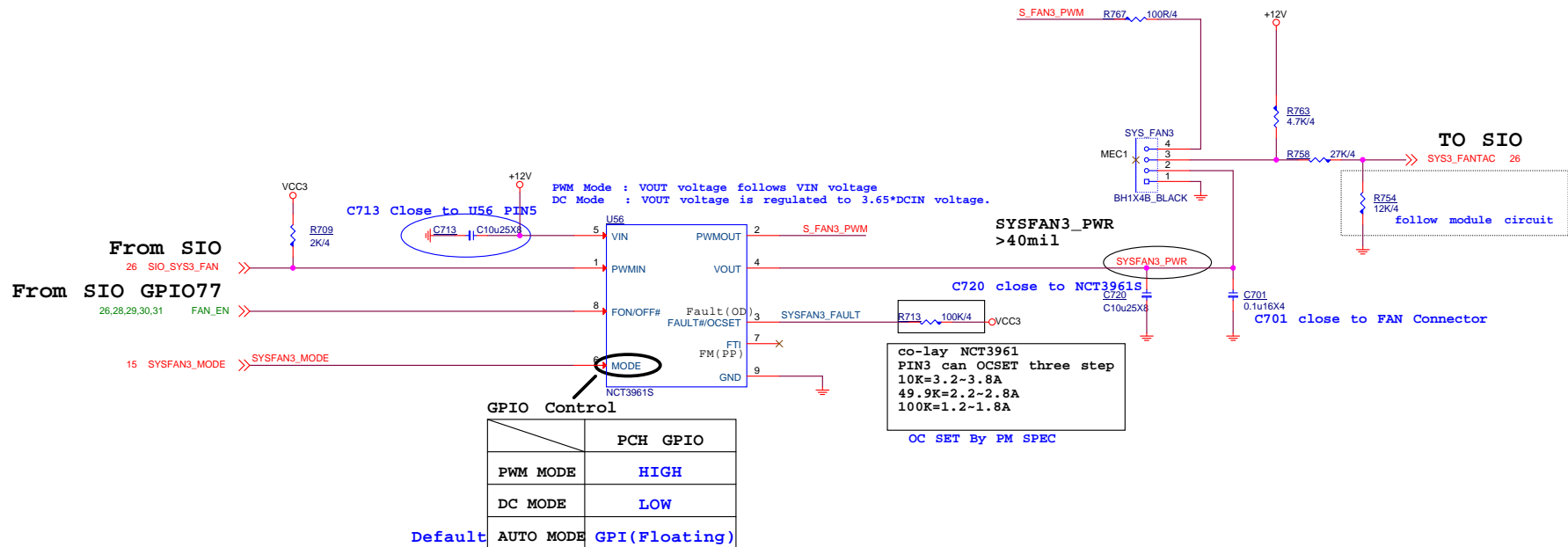
# TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



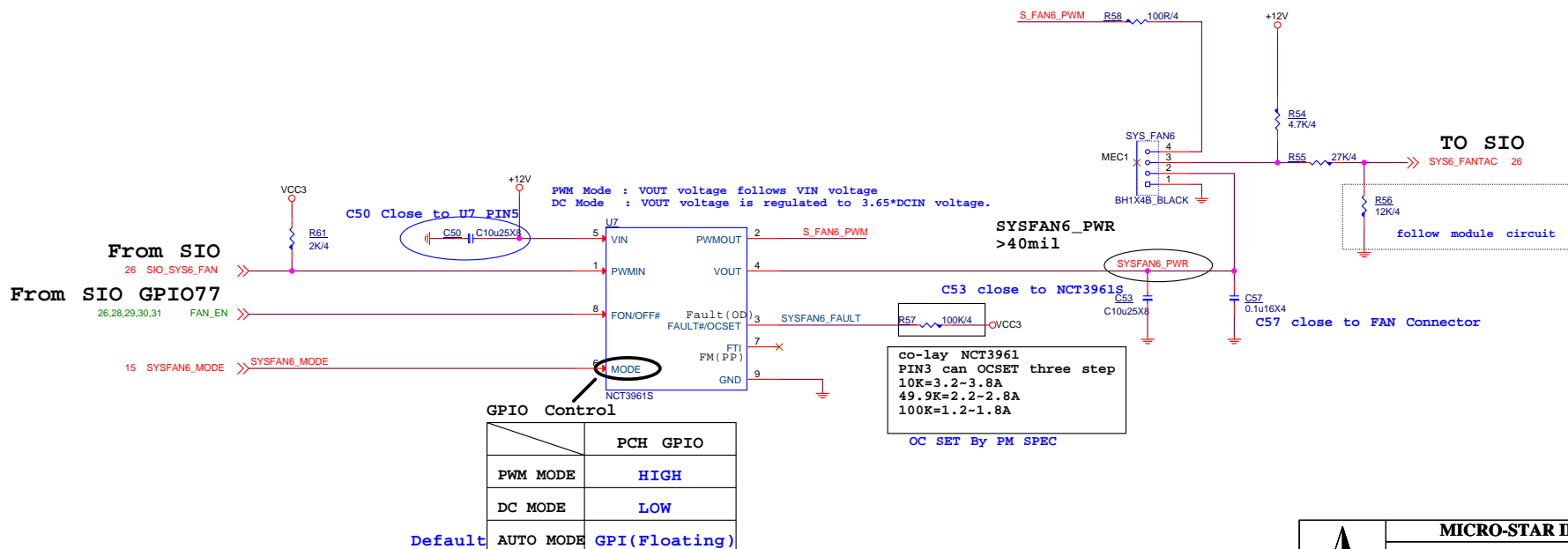
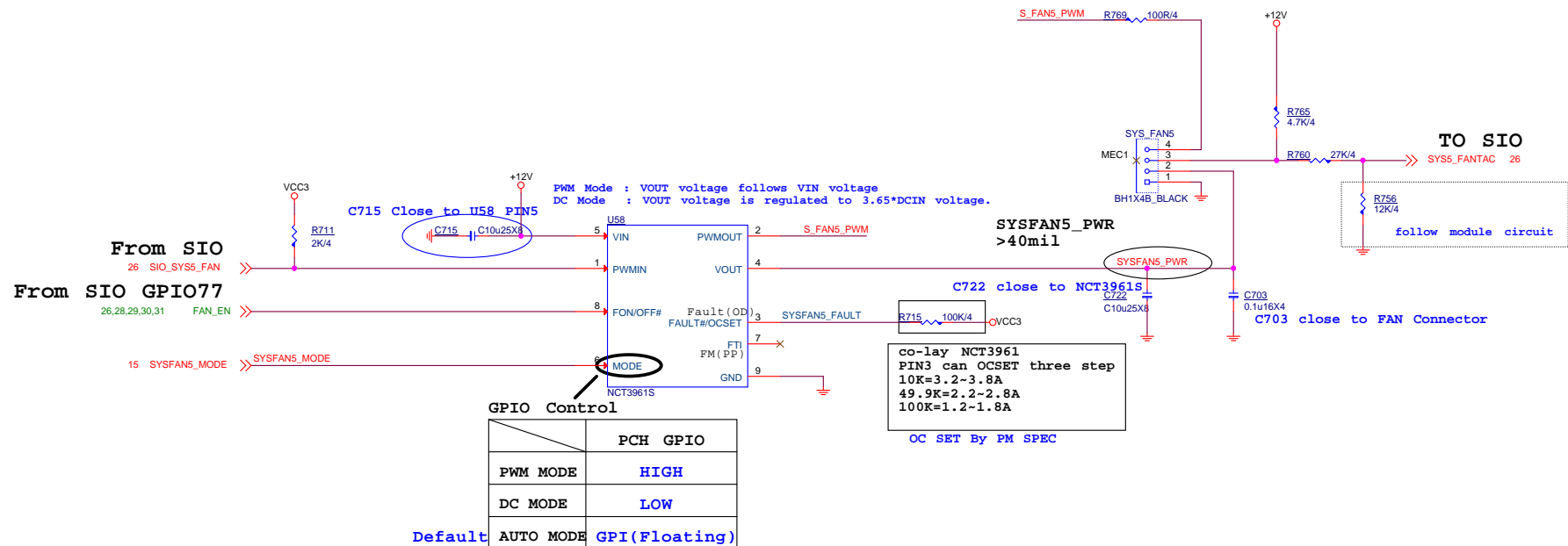
# TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

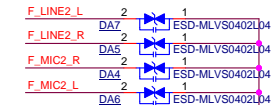
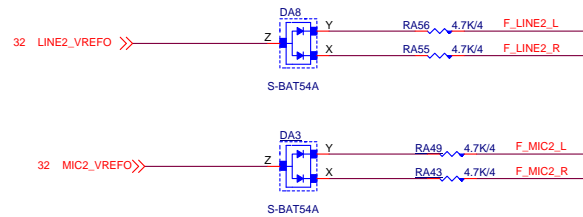
1.Mode GPIO BIOS can swtich PWM/DC MODE



# TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

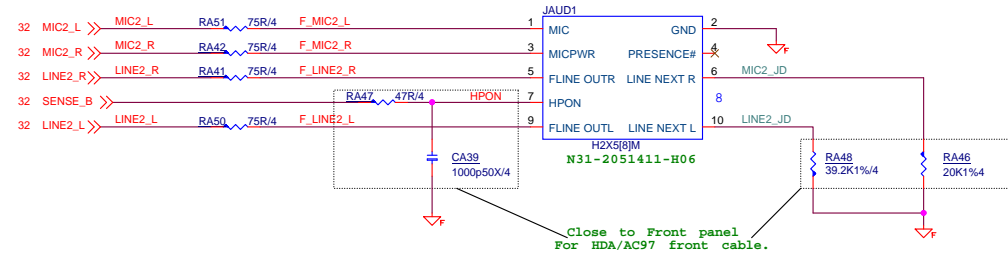
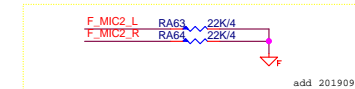
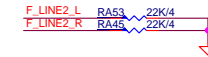
1.Mode GPIO BIOS can swtich PWM/DC MODE





ODG-7C71001-T43  
Close to Front panel

**ESD protect**  
D0G-2710510-I05  
AVL:ODG-7C71001-T43



De-POP circuit delete De-POP circuit at 20191218

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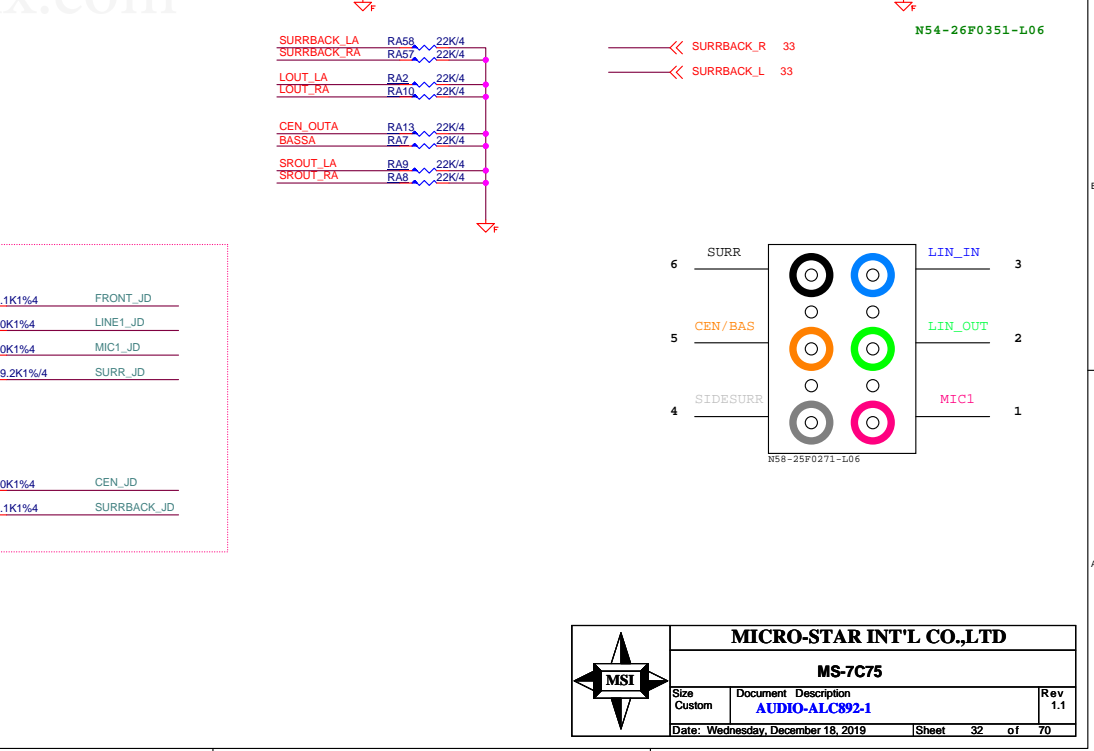
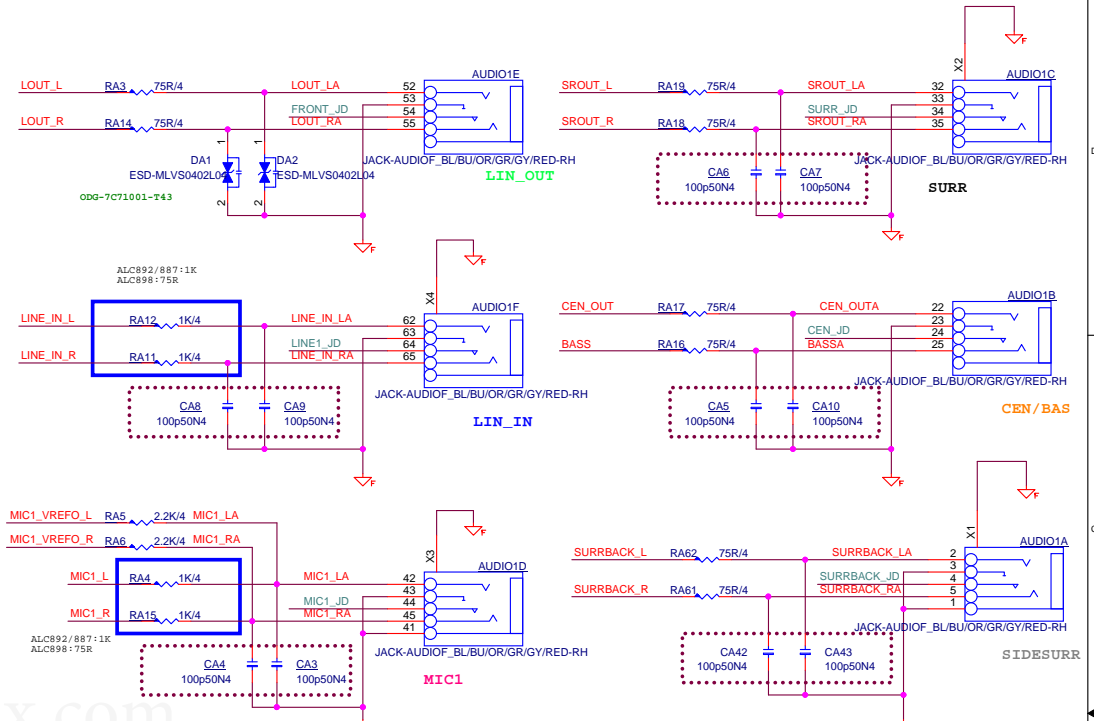
Vinafix.com

Vinafix.com

	MICRO-STAR INT'L CO.,LTD		
	MS-7C75		
	Size Custom	Document Description <b>AUDIO-ALC892-2</b>	Rev 1.1
	Date: Wednesday, December 18, 2019	Sheet 33	of 70



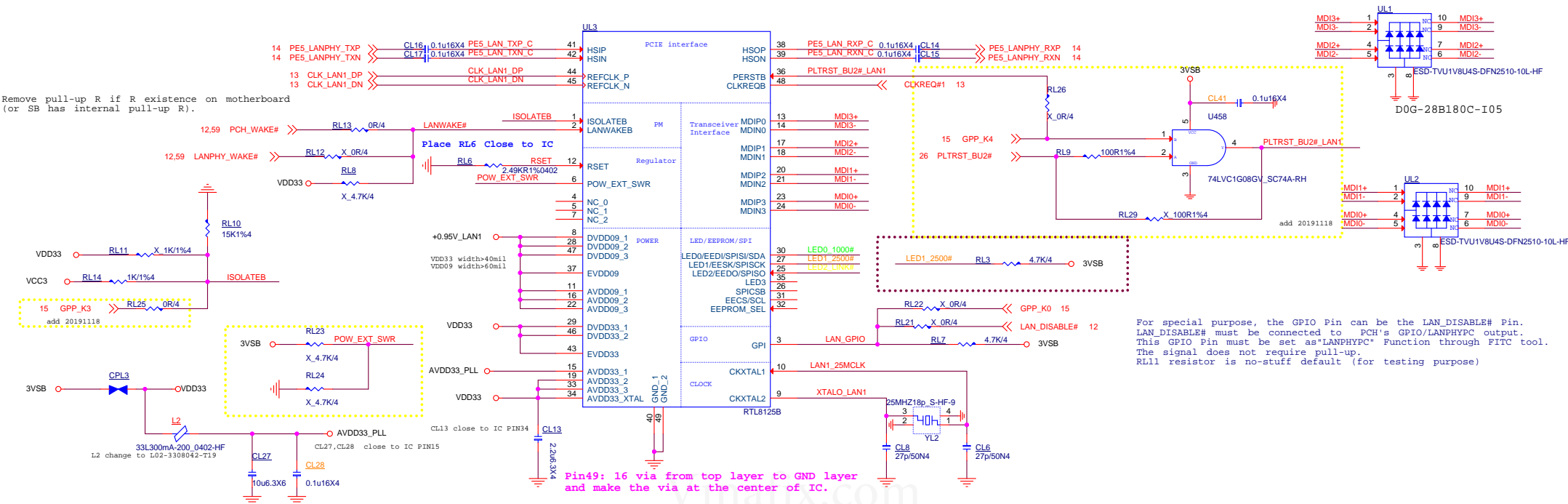
# ALC892



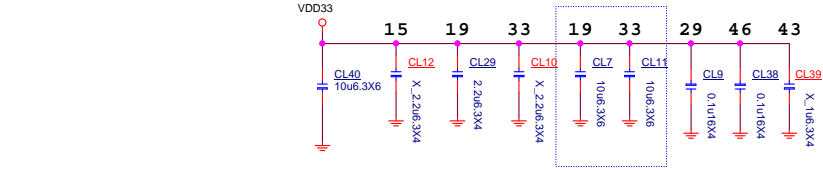
# RTL8125B 10/100/1000/2.5G LAN Controller

ESD Protect  
UL1&UL2 close to connector

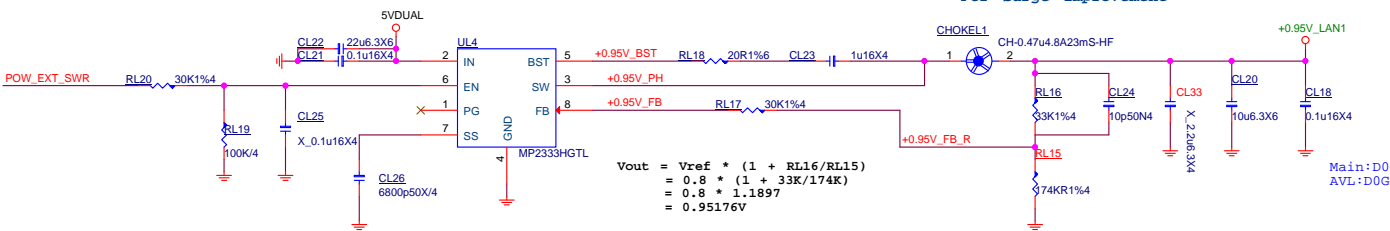
Remove pull-up R if R existence on motherboard  
(or SB has internal pull-up R).



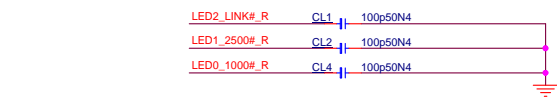
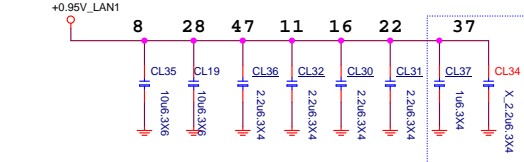
Place CL12, CL29, CL10, CL7, CL11, CL9, CL38, CL39 near Pin-15, 19, 33, 29, 46, 43



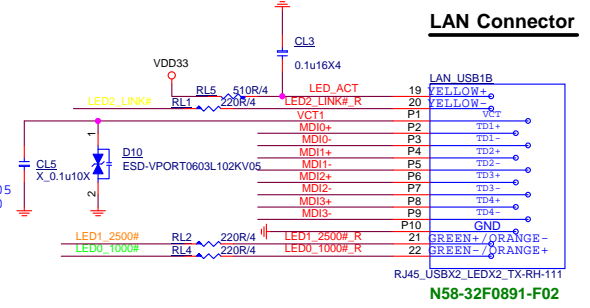
change to 5VDUAL 20191210



Place CL35, CL19, CL36, CL32, CL30, CL31, CL37, CL34 near Pin-8, 28, 47, 11, 16, 22, 37



## LAN Connector



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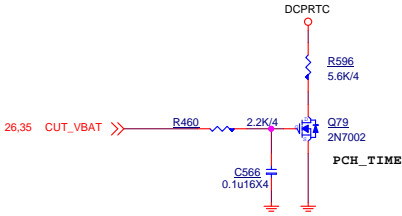
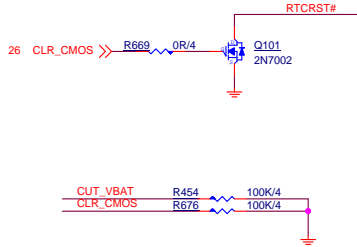
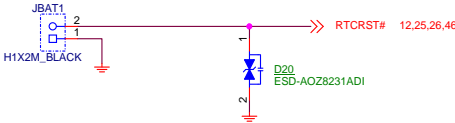
**MICRO-STAR INT'L CO.,LTD**

**MS-7C75**

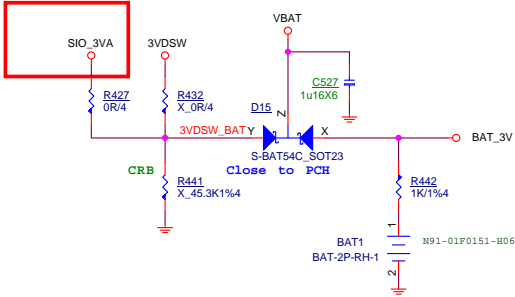
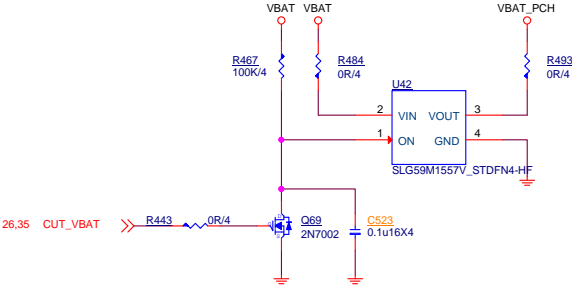
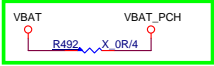
Size Custom Document Description  
**LAN RTL8125B**

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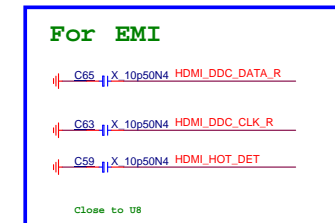
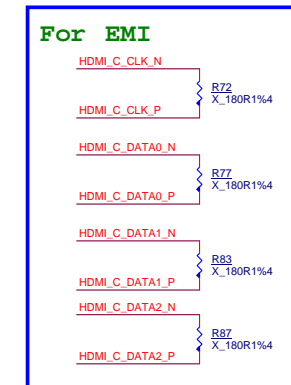
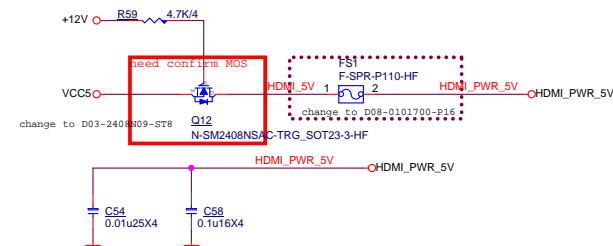
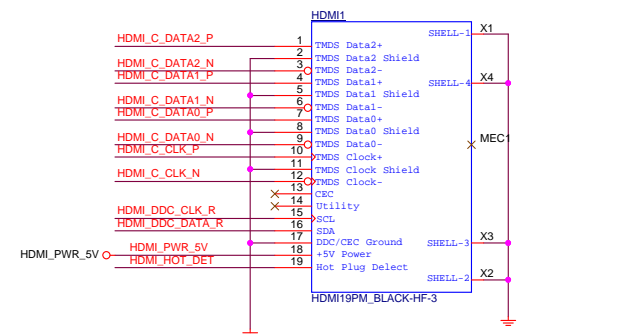
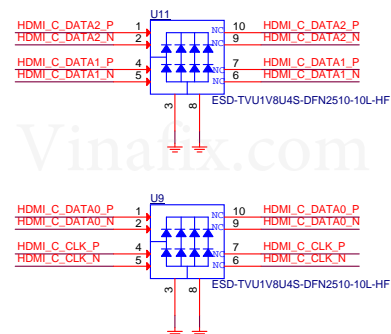
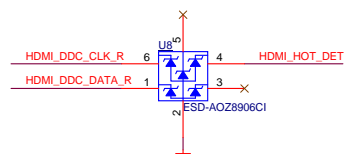
CUT\_VBAT/CLR\_CMOS

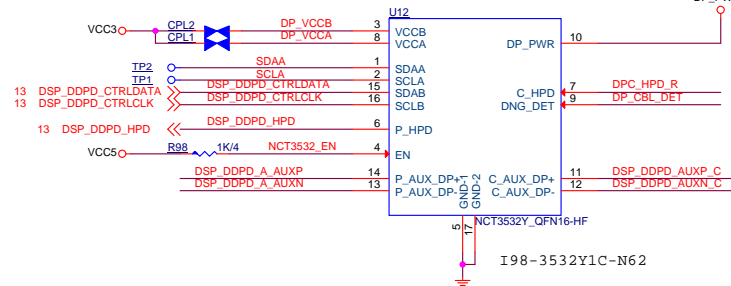
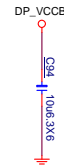
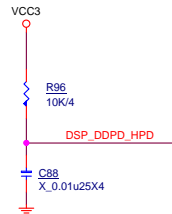
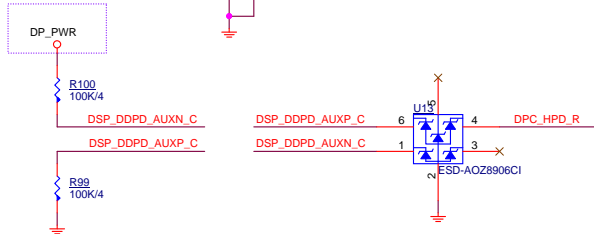
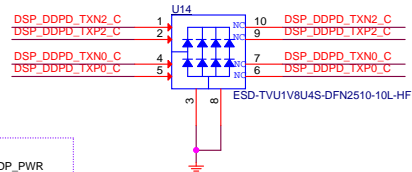
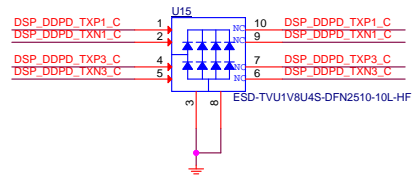


VBAT

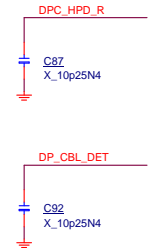
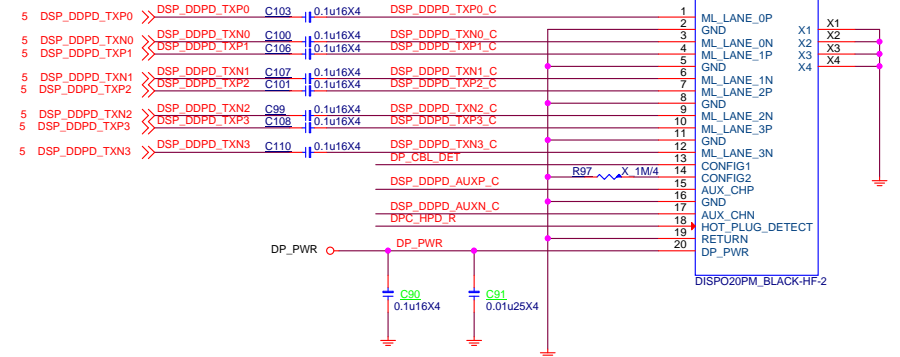


HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



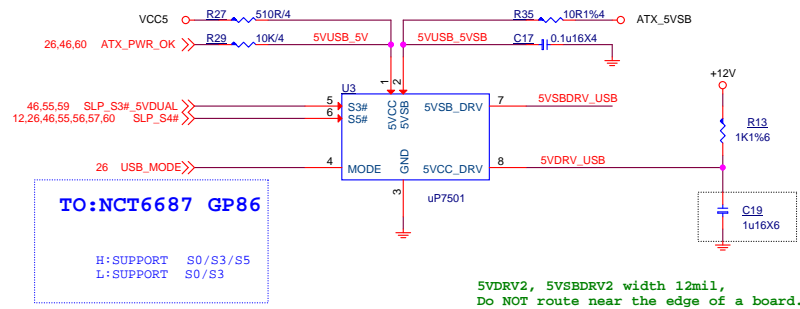


DP

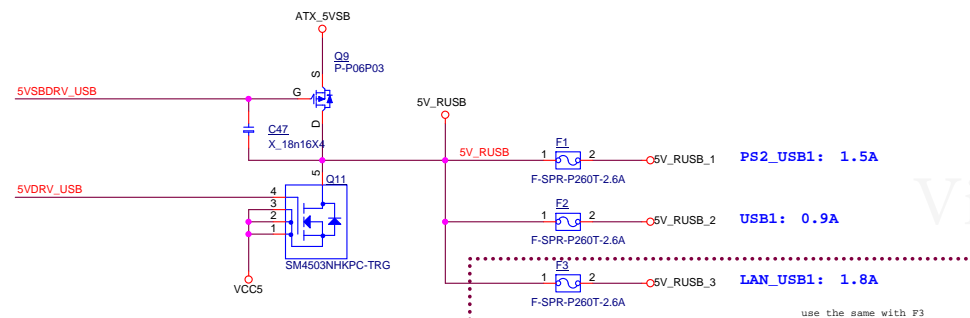


Vinafix.com  
DP\_VCCB trace don't less than 30 mil

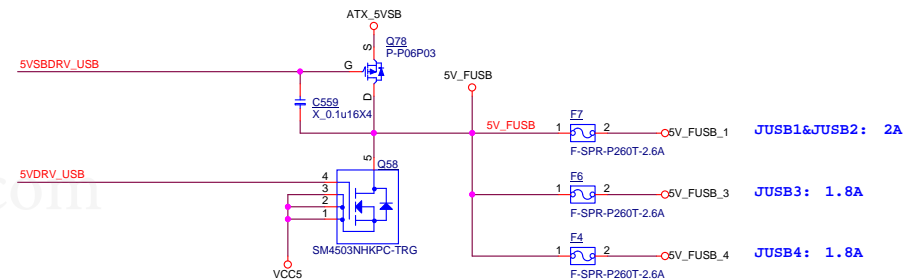
## USB Power



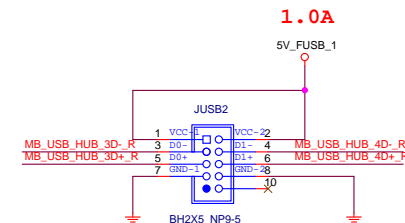
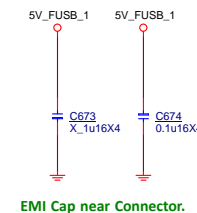
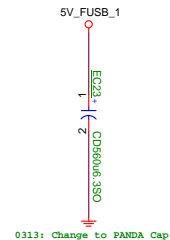
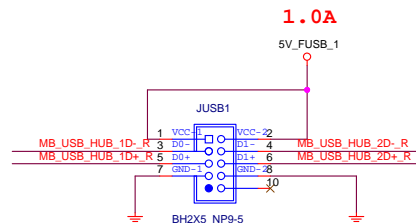
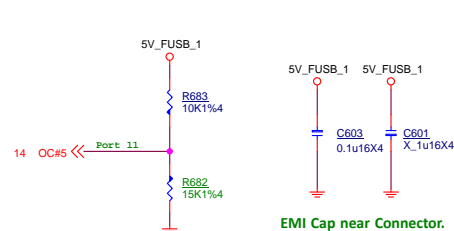
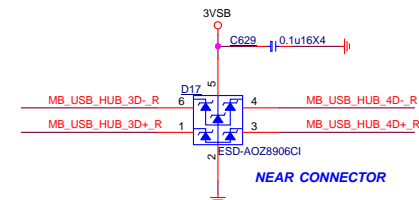
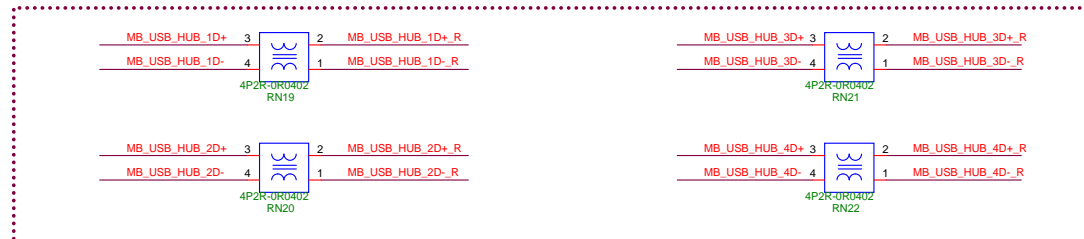
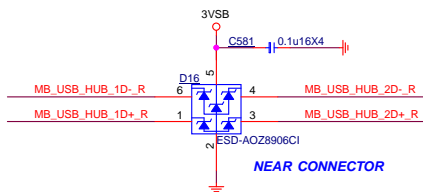
## Rear USB Port Power



### Front USB Port Power

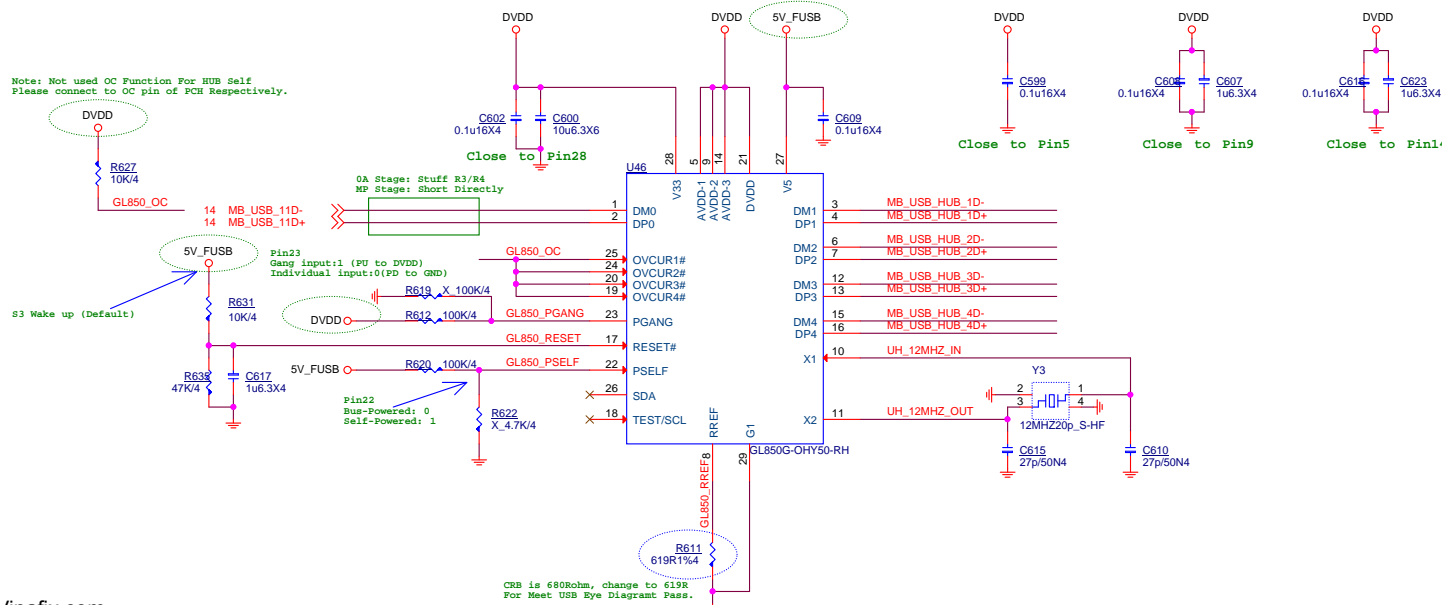


# Front USB2.0



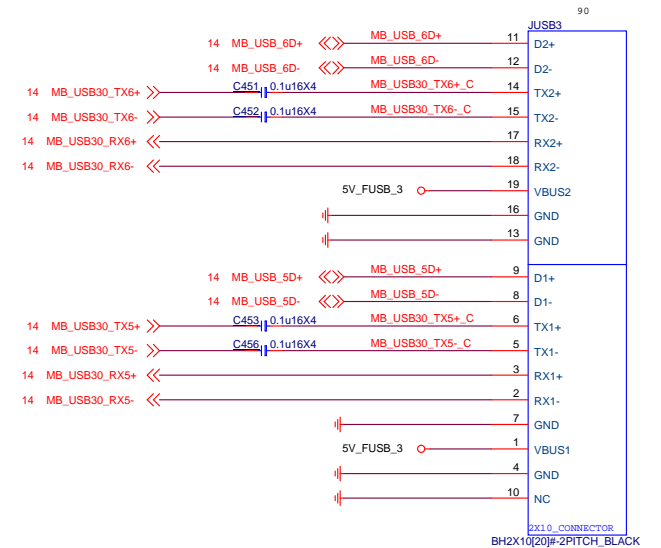
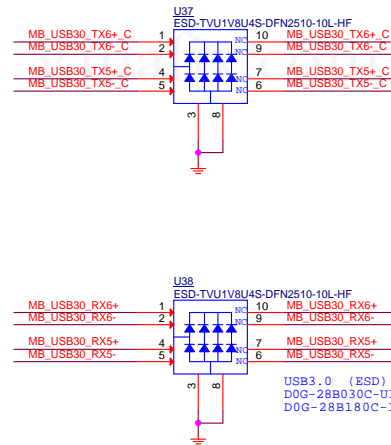
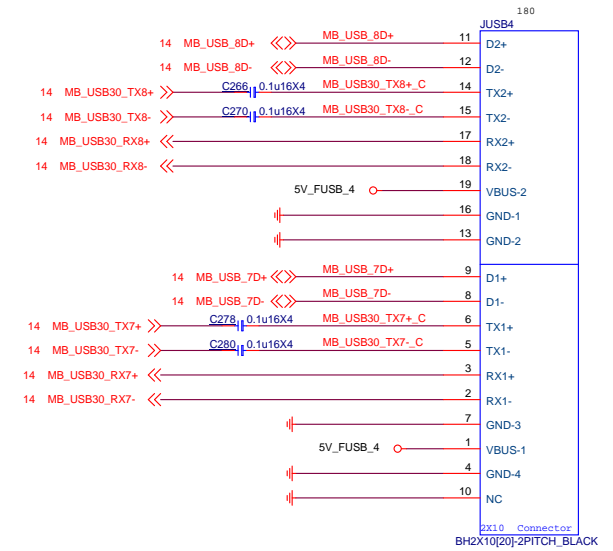
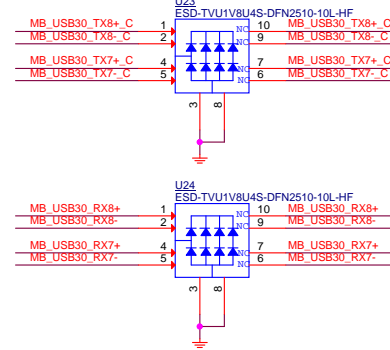
## GL850G USB2.0 HUB

Note: Please connect to USB Power Source.

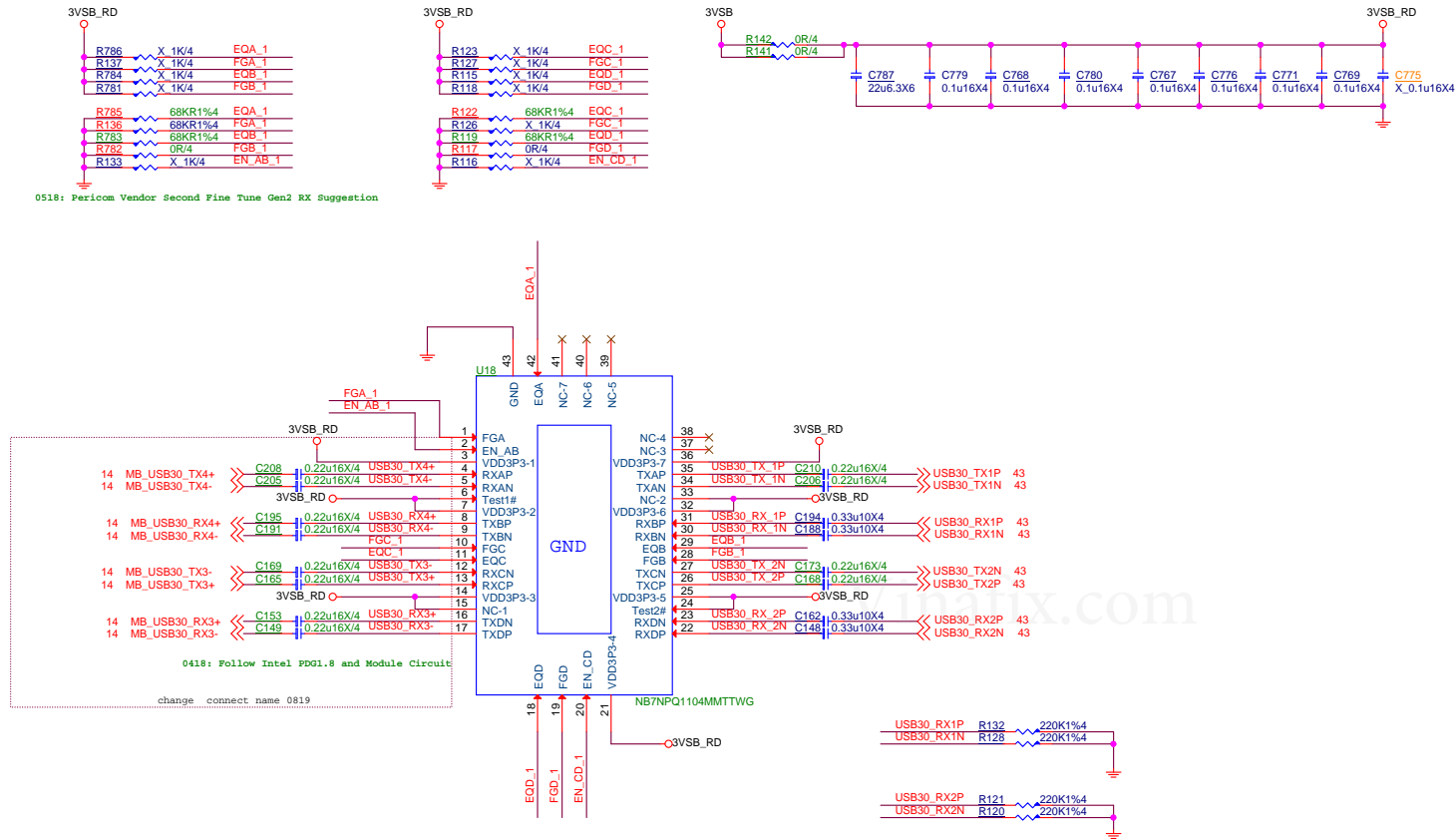




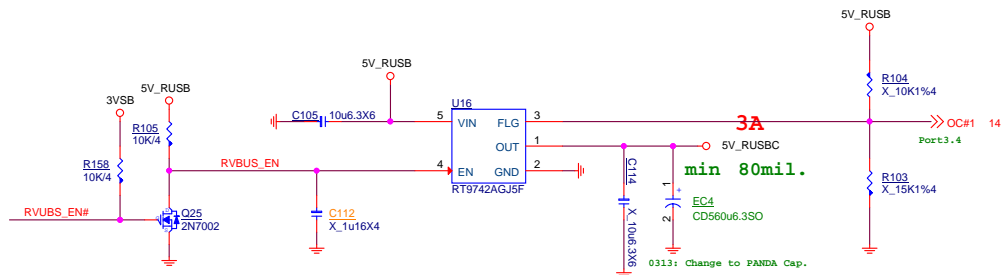
5	4	3	2	1
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## Rear USB3.1 Redriver



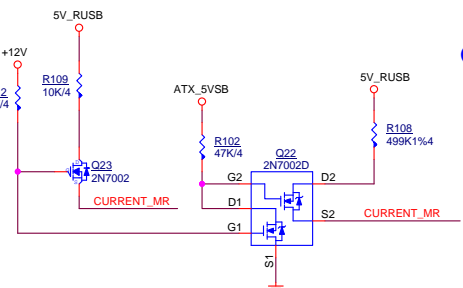
Vinafix.com



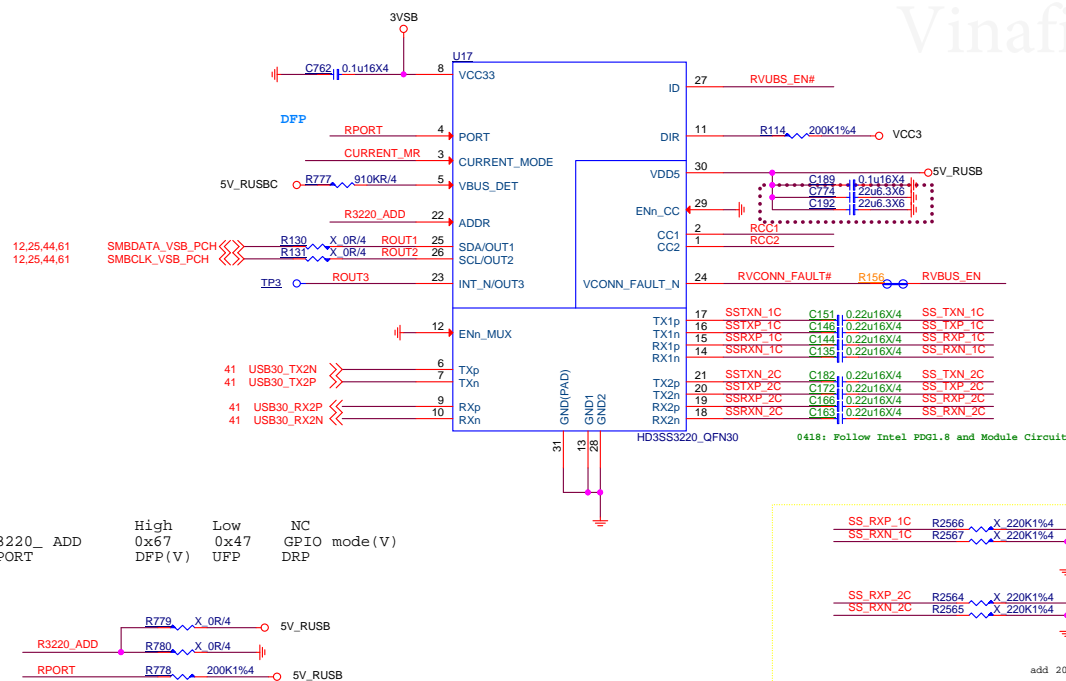
## Current Mode

3A under S0 mode  
1.5A under S3 mode

L - Default for 900mA  
M - Mid (500K) for 1.5A  
H - High (10K) for 3A

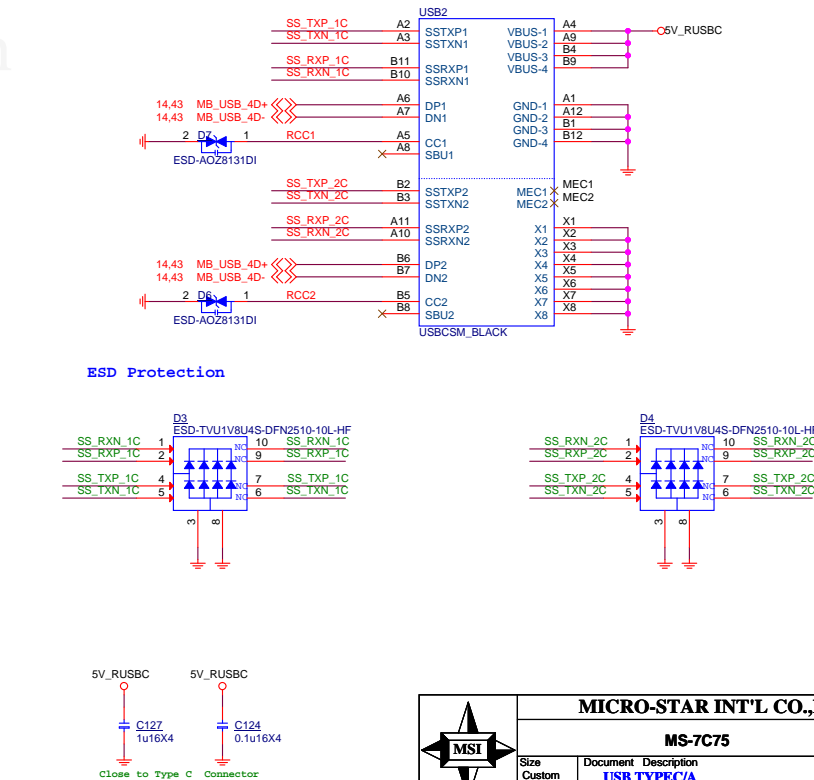


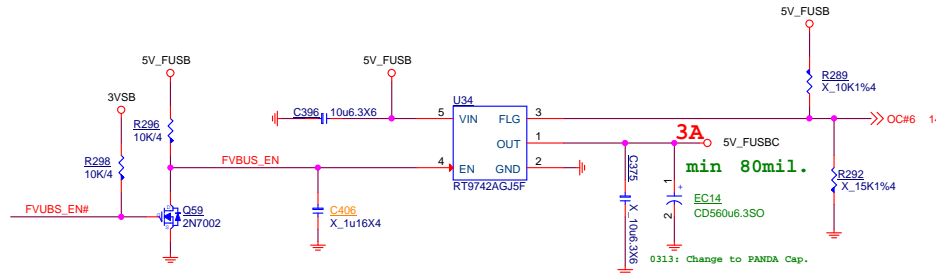
## USB Type-C MUX with Configuration Channel (CC)



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## TYPE-C

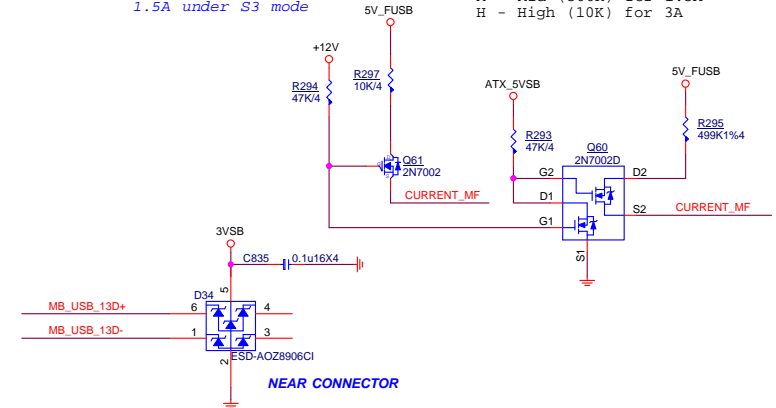




## Current Mode

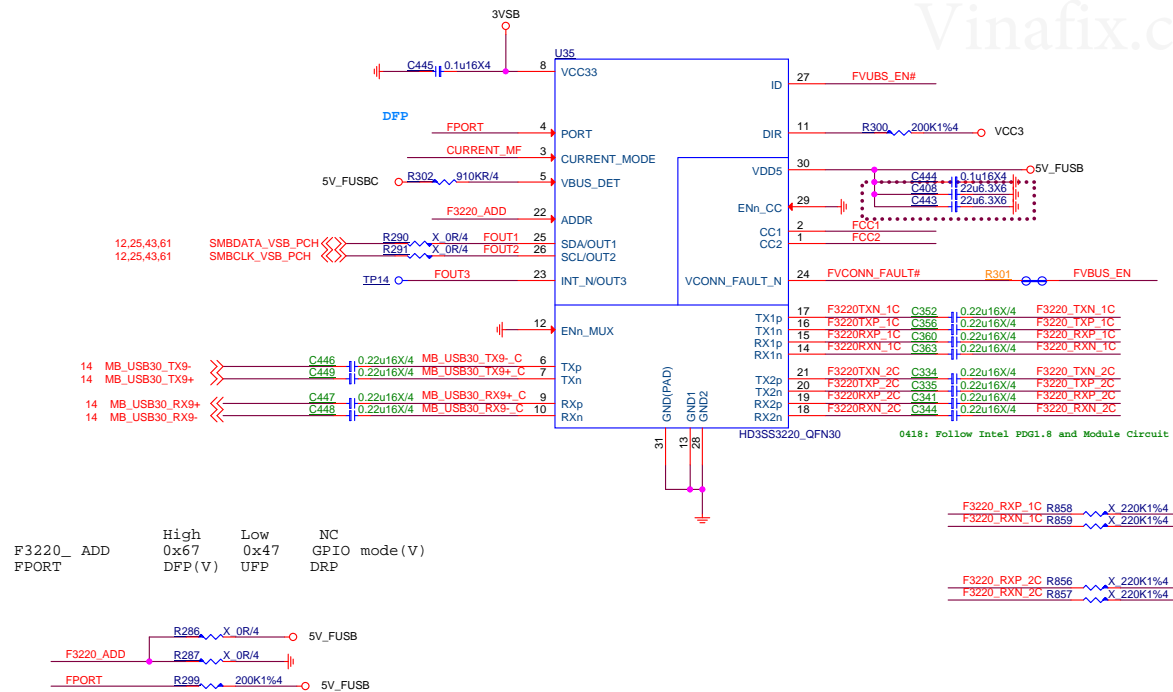
3A under S0 mode  
1.5A under S3 mode

L - Default for 900mA  
M - Mid (500K) for 1.5A  
H - High (10K) for 3A

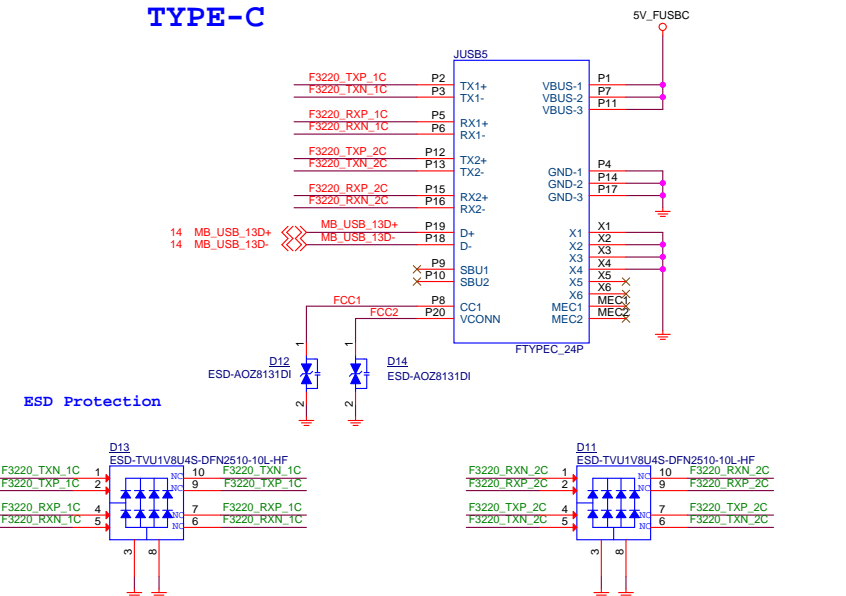


## USB Type-C MUX with Configuration Channel (CC)

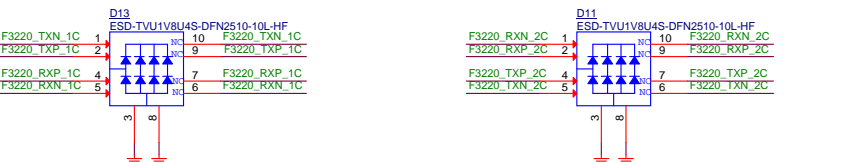
Vinafix.com



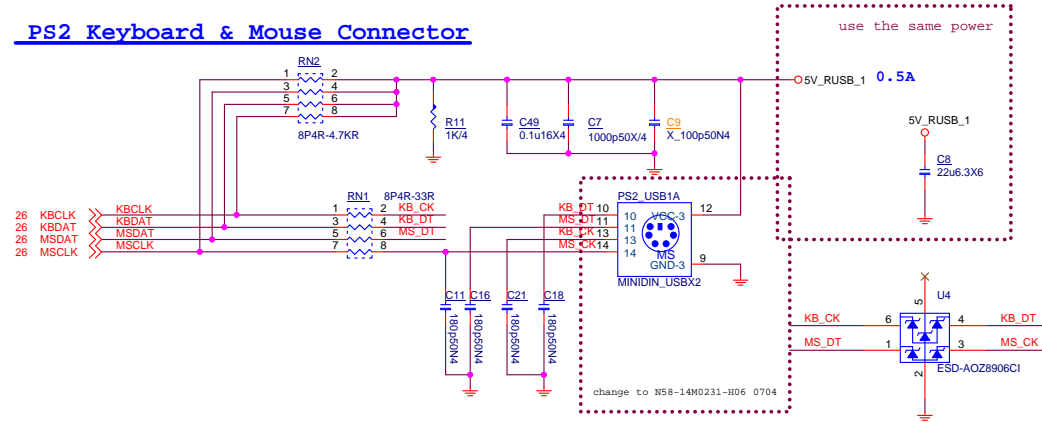
## TYPE-C



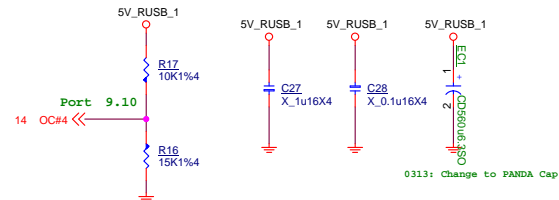
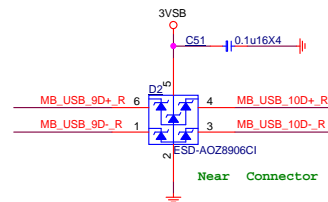
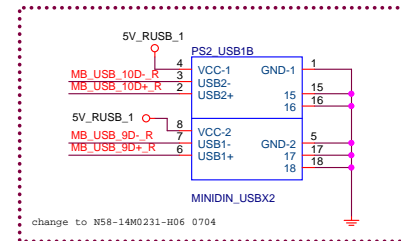
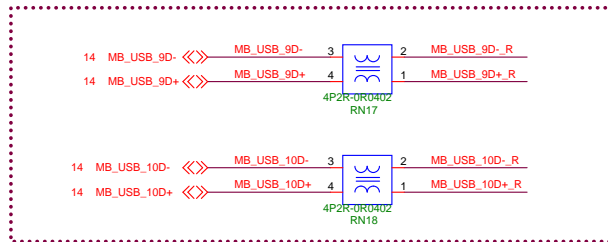
## ESD Protection



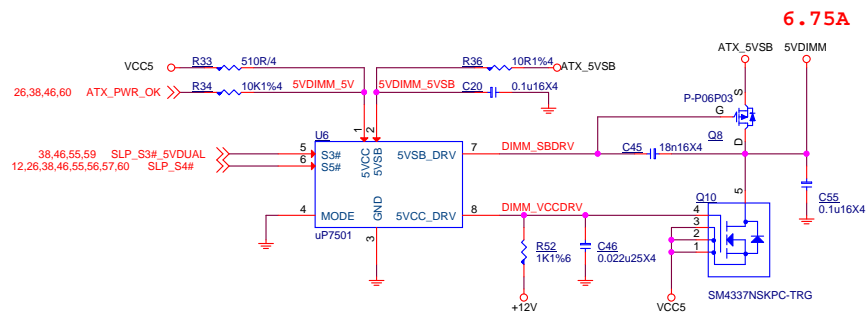
## PS2 Keyboard & Mouse Connector



## PS2 USB2.0

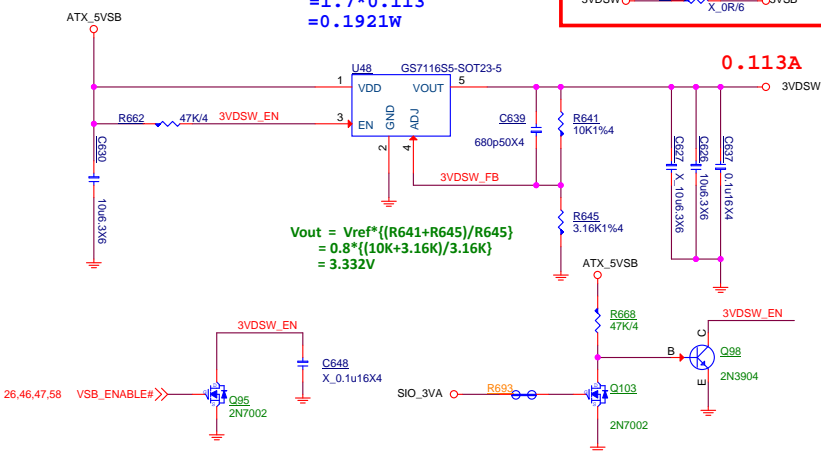


## 5VDIMM FOR DDR



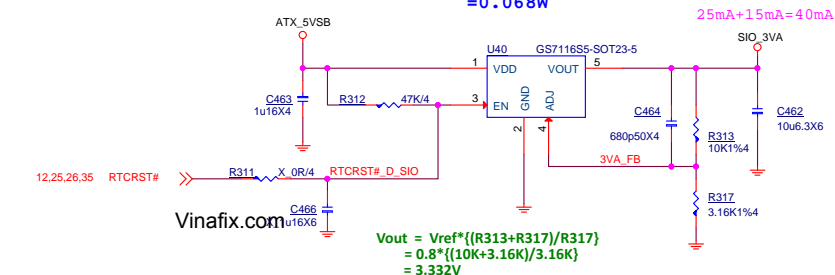
## 3VDSW

```
Power    Loss=(Vin-Vou)*Iout
          =(5-3.3)*0.113
          =1.7*0.113
          =0.1921W
```

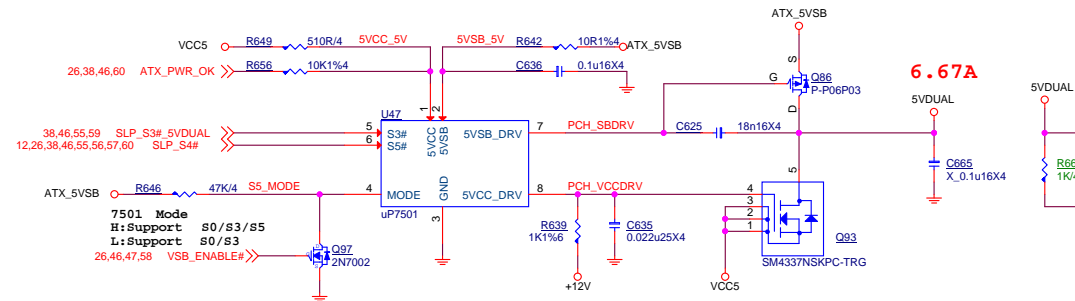


SIO\_3VA

```
Power    Loss=(Vin-Vou)*Iout
          =(5-3.3)*0.04
          =1.7*0.04
          =0.068W
```



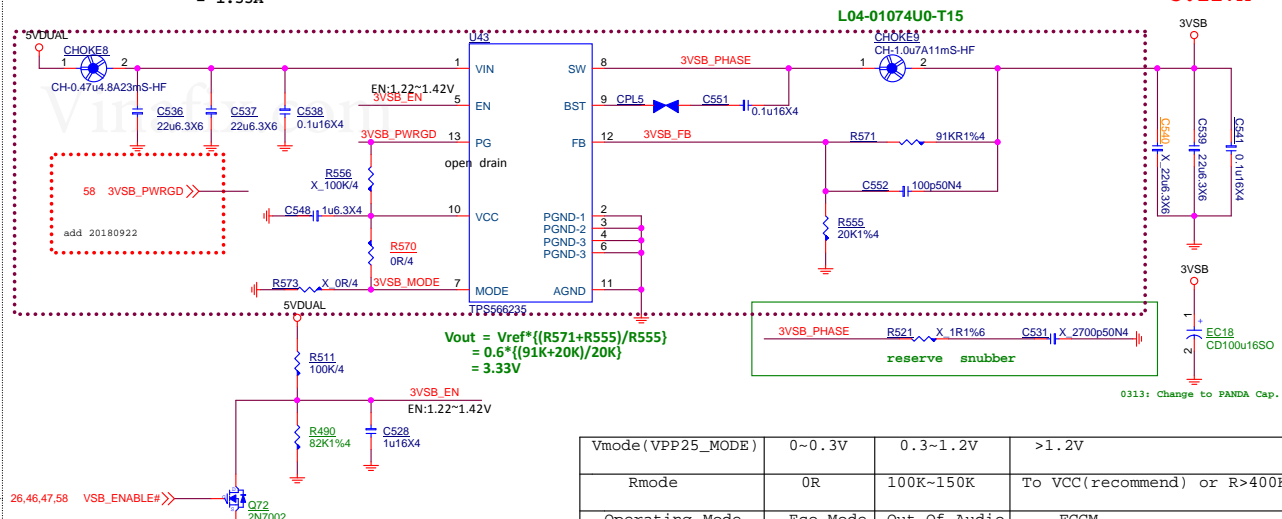
## 5VDUAL



3VSB

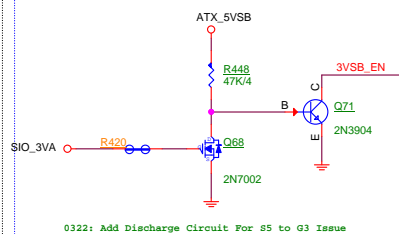
$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 3.227 * 0.474 \\ &= 1.53A \end{aligned}$$

) **Test OCP:8.4A**



Vmode(VPP25_MODE)	0~0.3V	0.3~1.2V	>1.2V
Rmode	0R	100K~150K	To VCC(recommend) or R>400K
Operating Mode	Eco-Mode	Out-Of-Audio	FCCM

For S5 -> G3 3VSB\_EN ISSUE



**MICRO-STAR INT'L CO.,LTD**

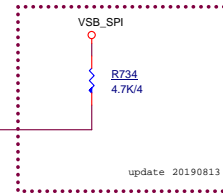
**MS-7C75**

Size Custom	Document <b>ACPI</b>
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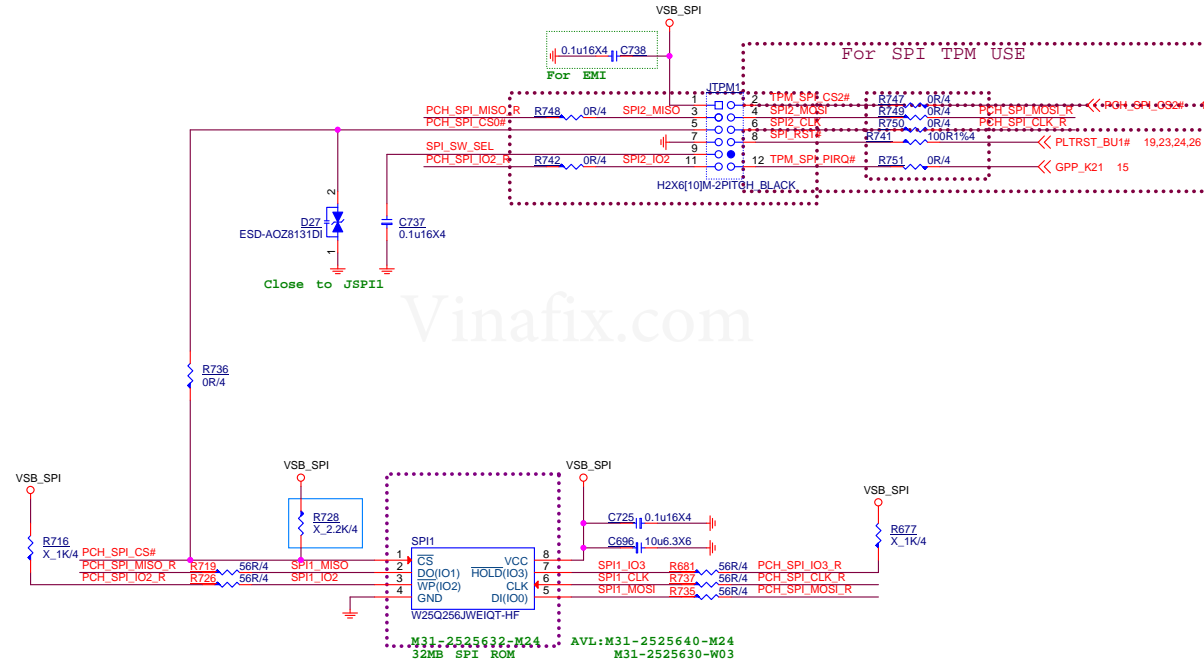
Rev	1.1
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12	PCH_SPI_CS0#	R729	0R/4	PCH_SPI_CLK_R
12	PCH_SPI_CLK	R718	0R/4	PCH_SPI_MOSI_R
12	PCH_SPI_MISO	R725	0R/4	PCH_SPI_MOSI_R
12,18	PCH_SPI_MOSI	R727	0R/4	PCH_SPI_IO2_R
12,18	PCH_SPI_IO2	R674	0R/4	PCH_SPI_IO3_R
12,18	PCH_SPI_IO3			

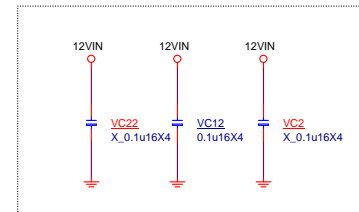
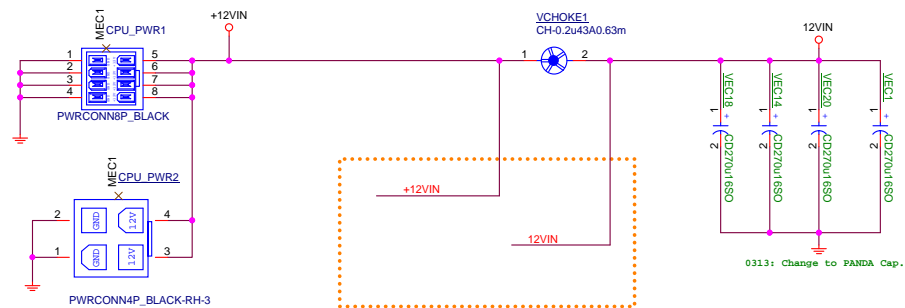
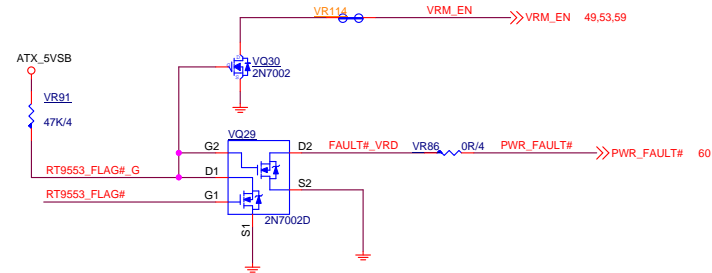
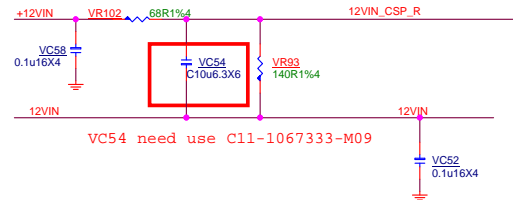
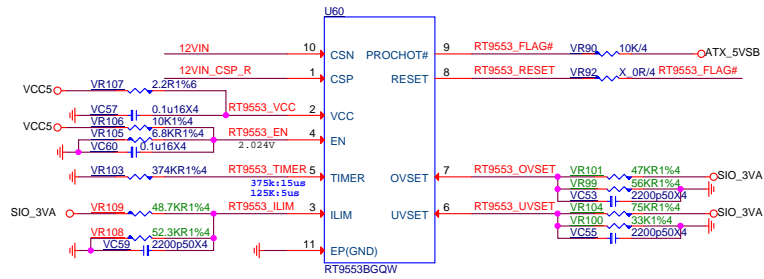


Pin 1 to 12 connection diagram for H2XG10M2PITGH\_BLACK. The diagram shows connections for VSB\_SPI, ITPM1, and various SPI signals. A dashed box labeled "For SPI TPM USE" encloses pins 1 through 12. Pin 1 is connected to PCH\_SPI\_MISO# and R748. Pin 2 is connected to PCH\_SPI\_CS0# and R749. Pin 3 is connected to SPI2\_MISO and R747. Pin 4 is connected to SPI2\_MOSI and R749. Pin 5 is connected to SPI2\_CLK and R750. Pin 6 is connected to SPI2\_CS1 and R747. Pin 7 is connected to SPI\_SW\_SEL and R742. Pin 8 is connected to PCH\_SPI\_IO2 and R742. Pin 9 is connected to SPI2\_IO2 and R742. Pin 10 is connected to TPM\_SPK\_PIRQ# and R751. Pin 11 is connected to TPM\_SPK\_PIRQ# and R751. Pin 12 is connected to TPM\_SPK\_PIRQ# and R751. A note "H2XG10M2PITGH\_BLACK" is at the bottom. A note "For EMI" is near the VSB\_SPI connection. A note "For SPI TPM USE" is in a dashed box around the main connections.



	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7C75</b>		
	Size Custom	Document Description <b>BIOS ROM</b>	Rev 1.1
	Date: Thursday, January 02, 2020		Sheet 47 of 70

OCP: 45A For 10 core 245A Support



3.53 VR\_VIDSOUT << VR\_VIDSOUT VR27 X 100R1%4  
3.53 VR\_VIDSClk << VR\_VIDSClk VR32 X 45.3R1%4  
3.53 VR\_VIDALERT# << VR\_VIDALERT# VR29 X 0R/4  
VR\_HOT# VR33 X 301R1%4



I2C Address:0x21

Register	Default	Thermal
PHASE1	0x00	4
PHASE2	0x01	4
PHASE3	0x02	4
PHASE4	0x03	4
PHASE5	0x04	4
PHASE6	0x05	4

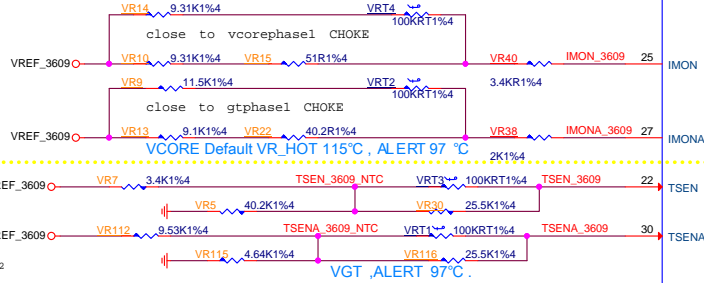
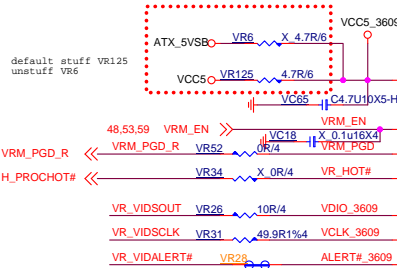
If high change to small, low change to big. cannot exceed '7'

	Register	Default
SVID Alert#_VCORE	0x06	6 (97°C)
SVID Alert#_VGT	0x42	6 (97°C)

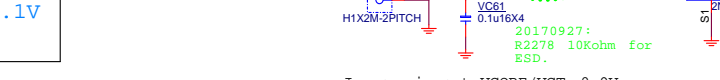
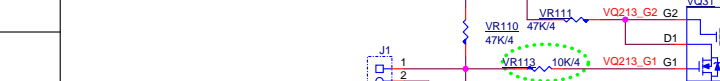
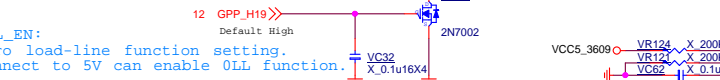
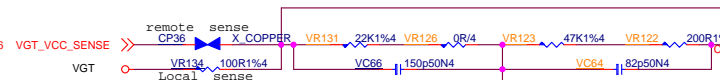
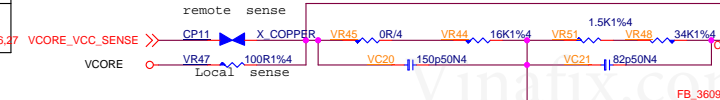
TSEN:SET Iccmax for VCore,  
SVID Alert#,Vr\_hot#.  
TSENA:SET Iccmax for VGT,  
SVID Alert#,Vr\_hot#.

I2C Address:0x21

	Register	VBOOT	VBOOT
VCORE	0x13	83	A5
	0x14	00	00
	0x12	01	01
	0x53	83	A5
VGT	0x54	00	00
	0x52	01	01

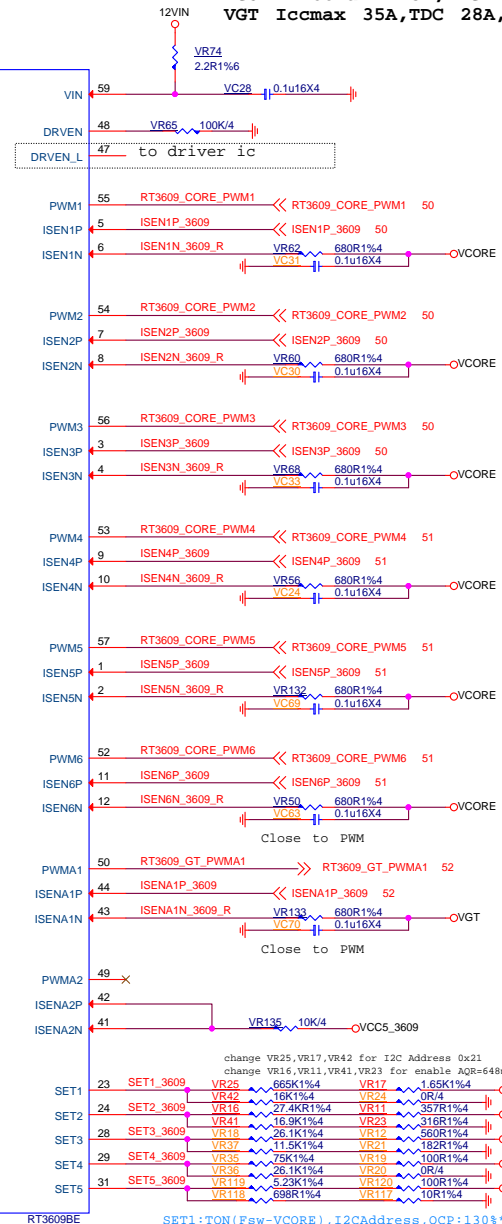


modify 20190912

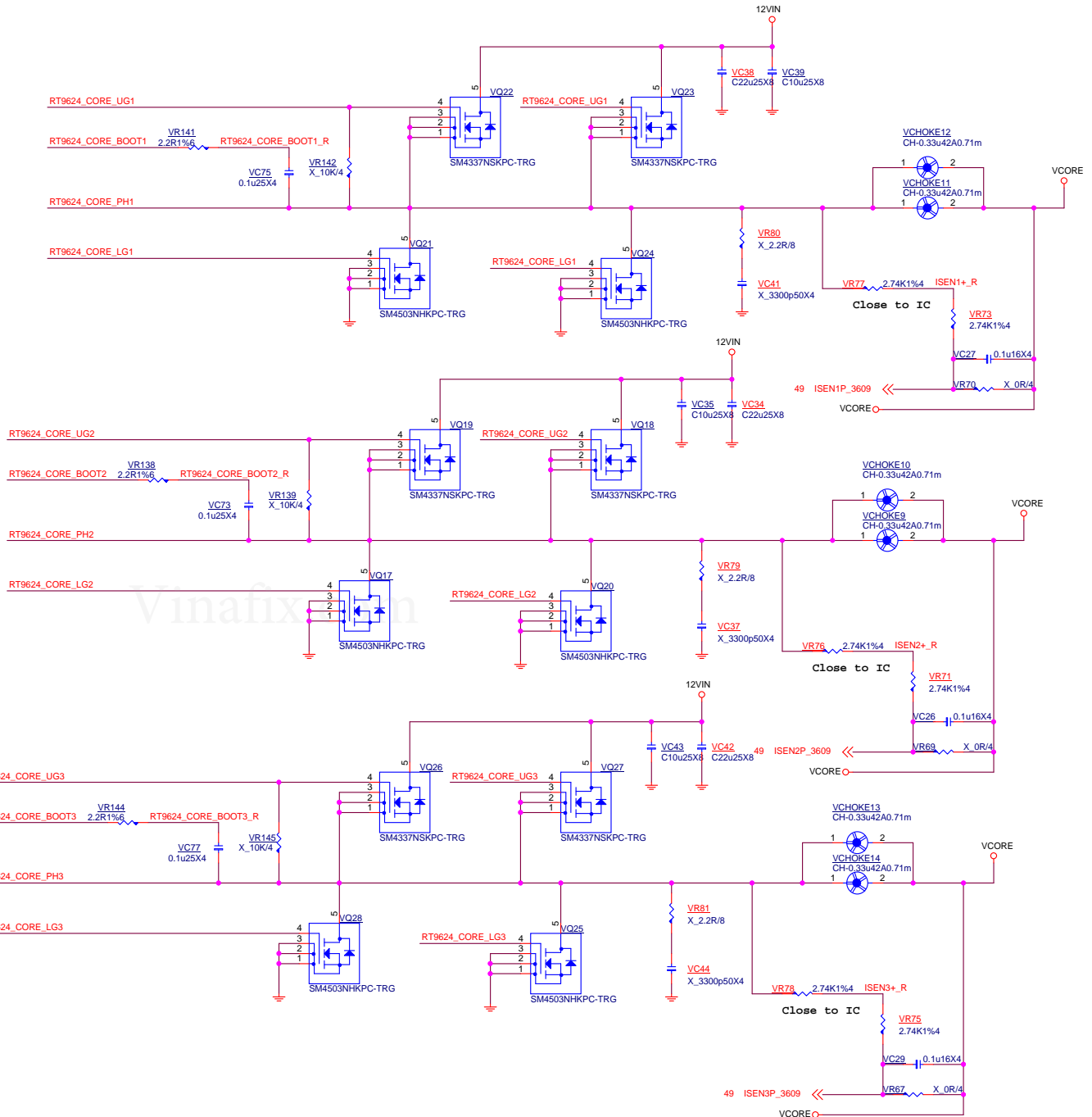
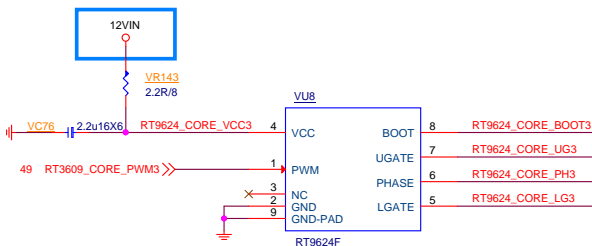
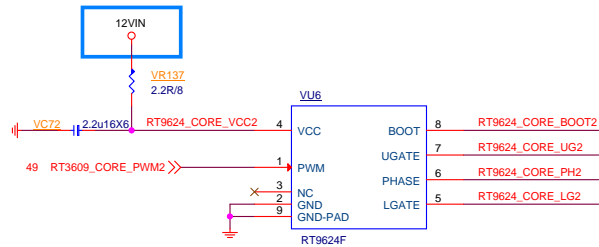
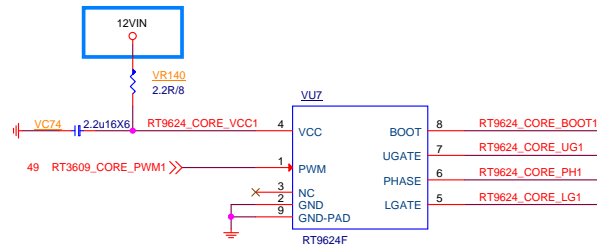


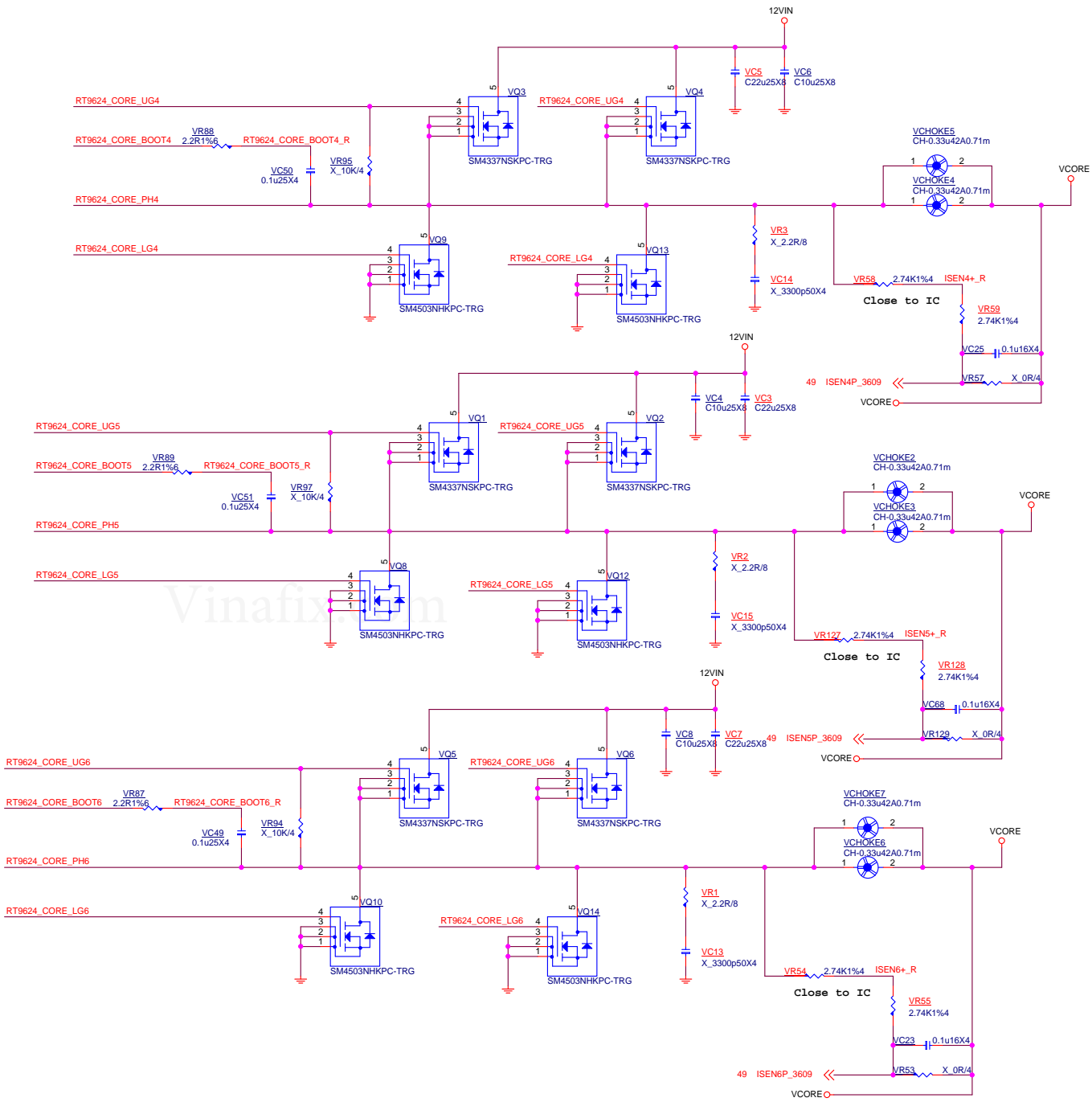
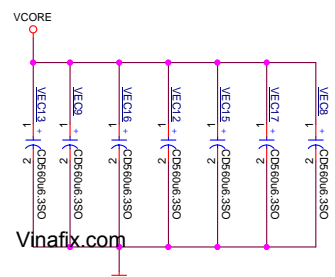
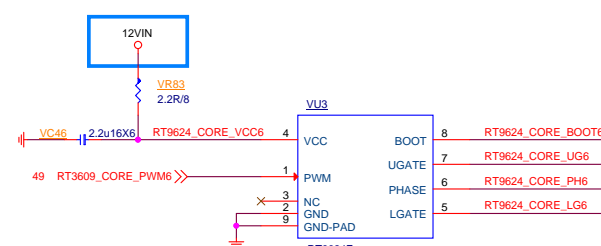
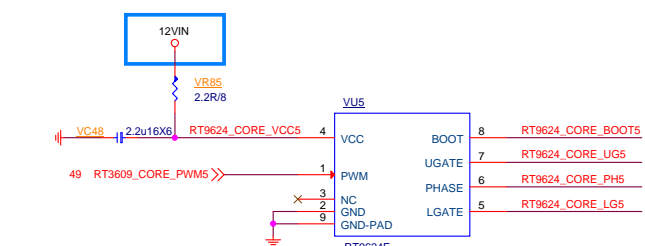
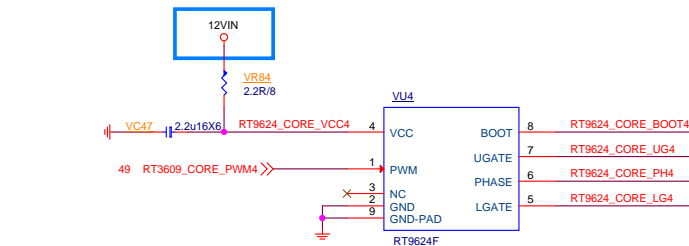
Jumper insert,VCORE/VGT 0.9V.

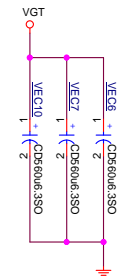
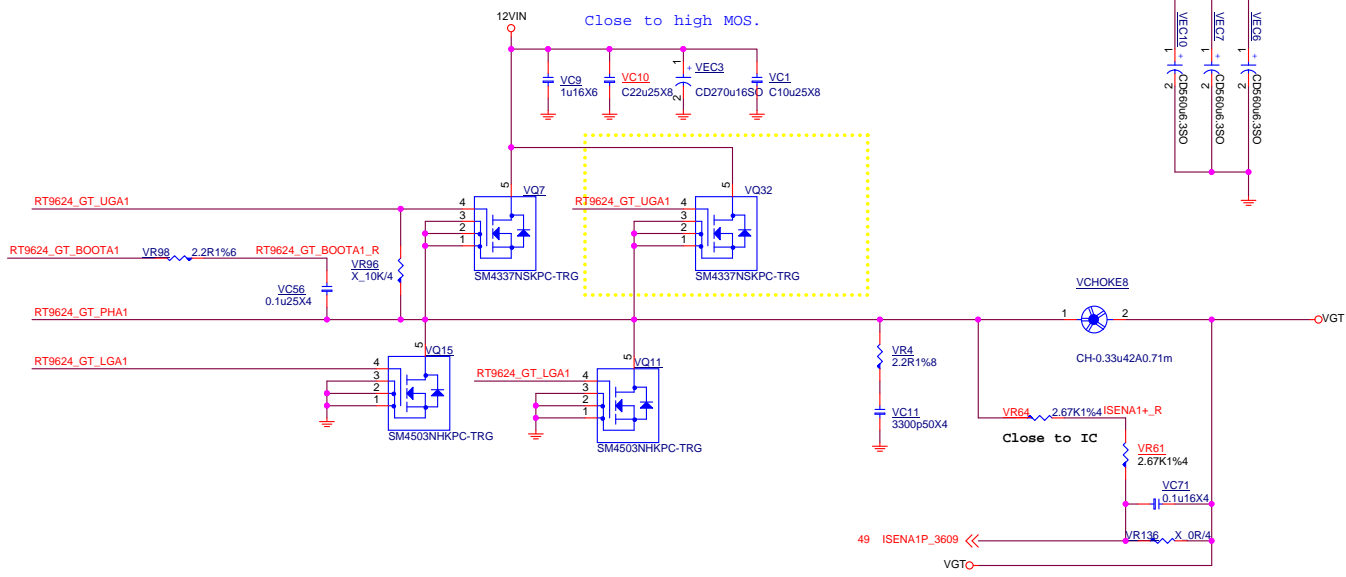
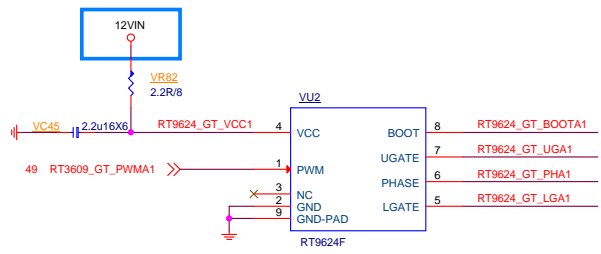
VCORE Iccmax 245A,TDC 175A, OCP318A.  
VGT Iccmax 35A,TDC 28A, OCP45A.



SET1:TON(Fsw-VCORE),I2CAddress,0CP:130\*Iccmax(VCORE).  
SET2:AQR trigger level for VCore.  
Advanced ramp magnitude in PS0 for VCore.  
SET3:Adaptive ramp trigger level in PS1/PS2/PS3 for VCore.  
Adaptive ramp trigger level in PS0 for GT.  
DVID voltage compensation level for VCore and GT.  
SET4:AQR trigger level for GT.  
Advanced ramp magnitude in PS0 for GT.  
SET5:TON(Fsw-GT),0CP:130\*Iccmax(GT),Zero LL.  
DVID fast slew rate 12.8mV/us.

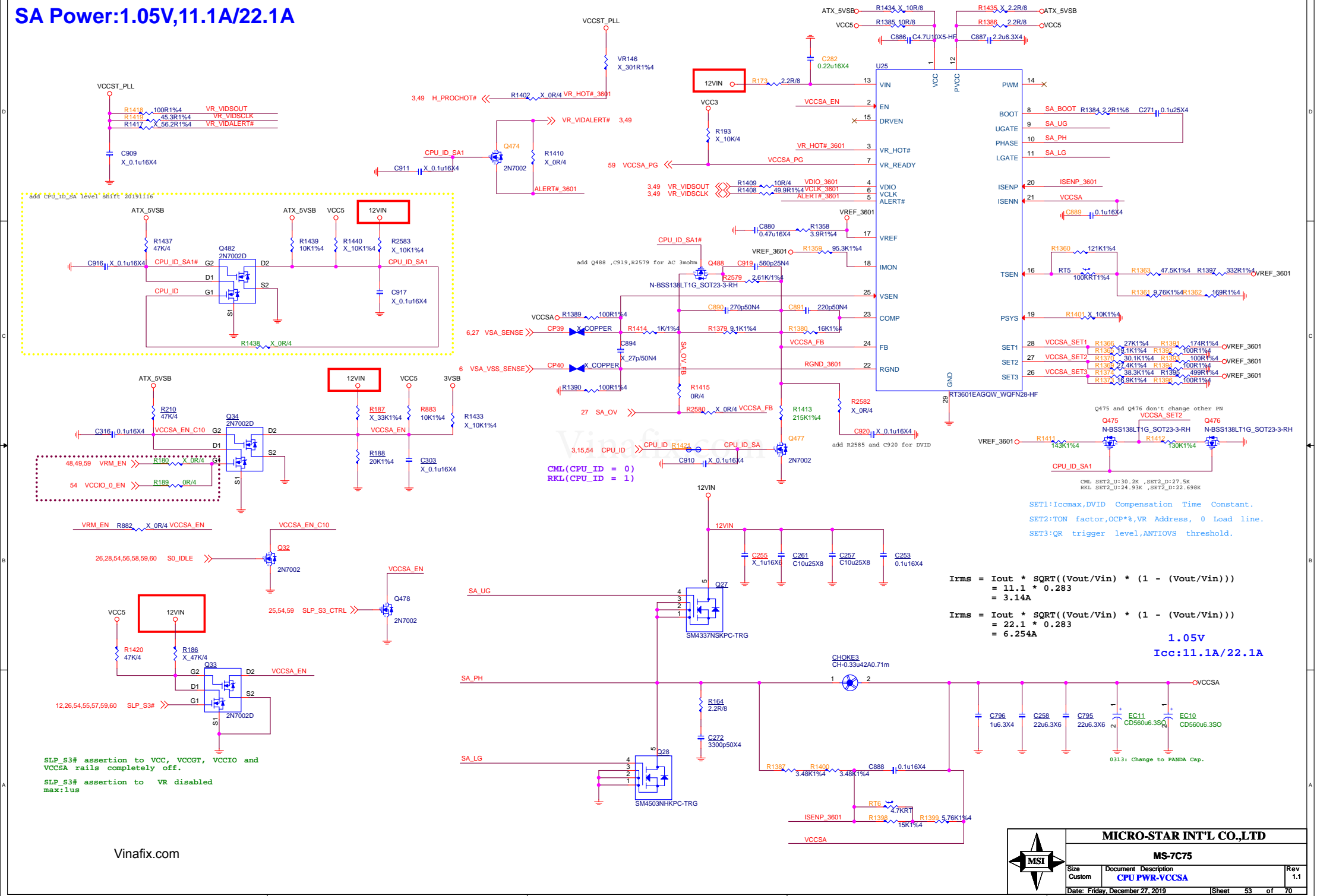






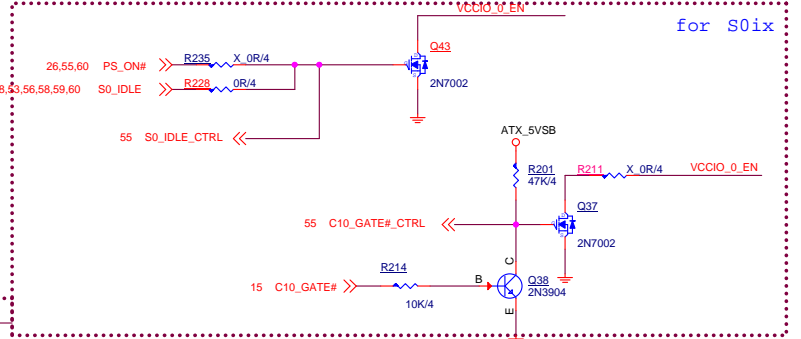
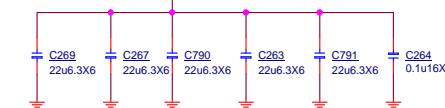
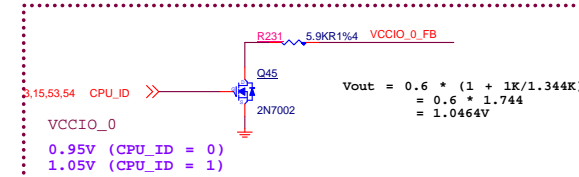
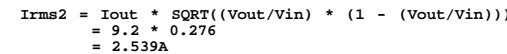
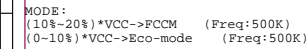
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**SA Power:1.05V,11.1A/22.1A**



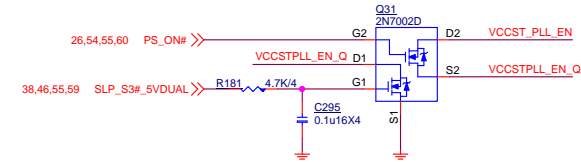
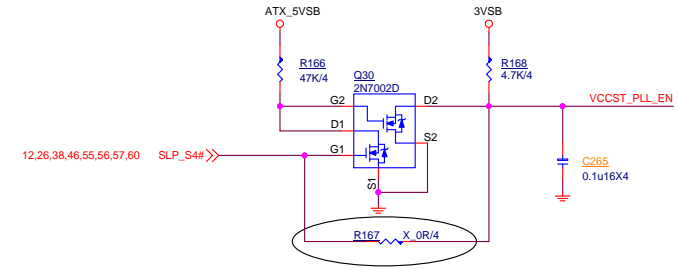
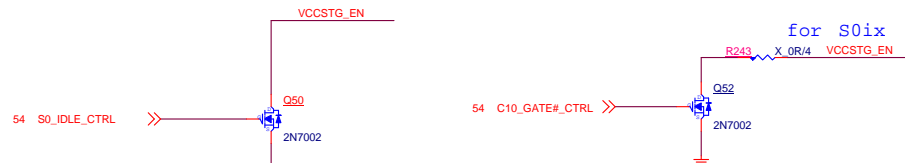
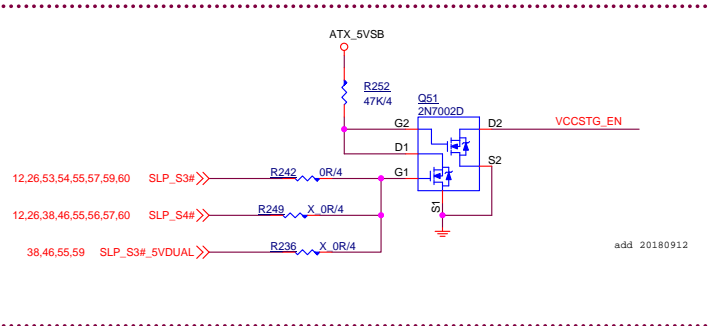
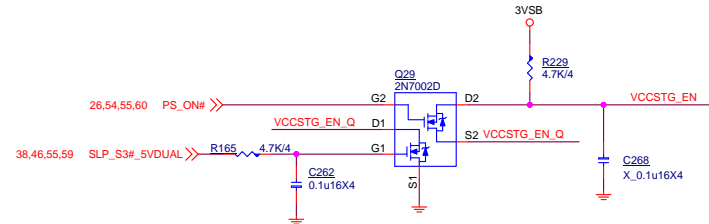
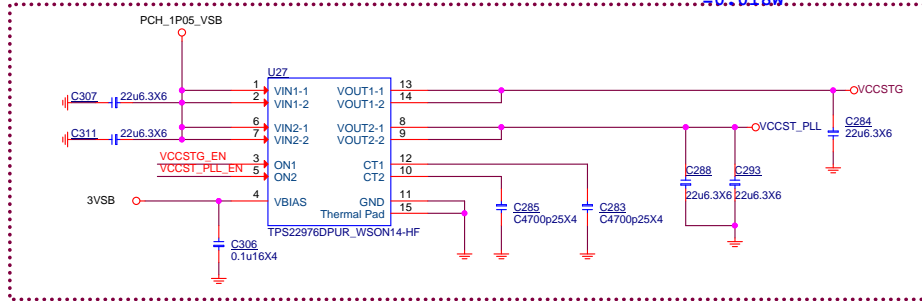


## VCCIO\_12 Power

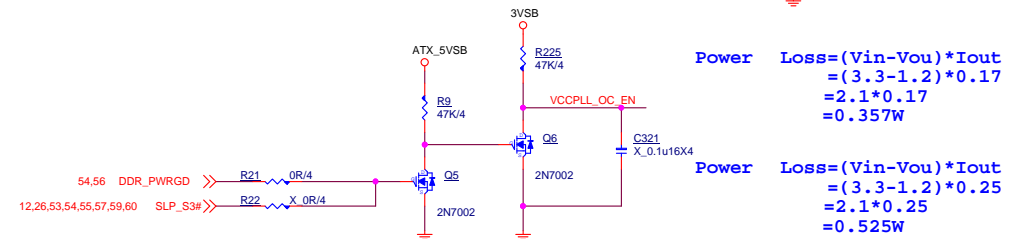
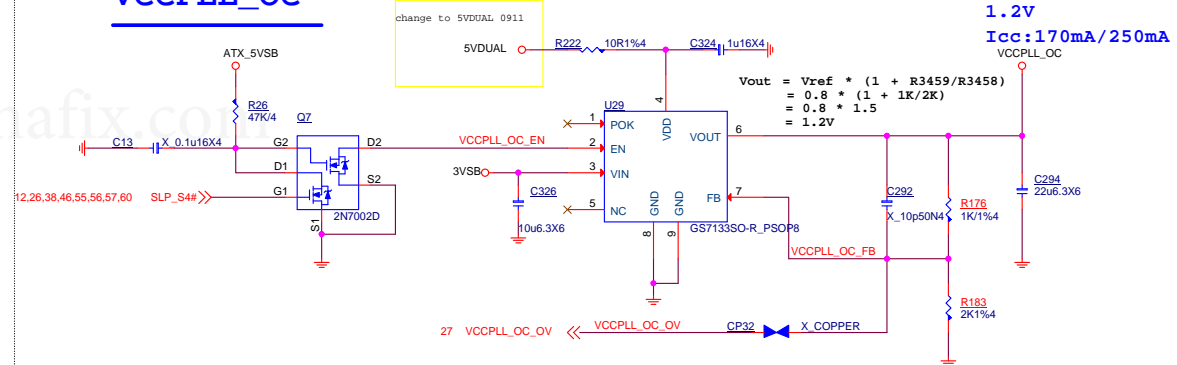


**VCCST\_PLL** 1.05V; 1.15A/2.53A  
**VCCSTG** 1.05V; 0.2A/0.9A

$$\begin{aligned} \text{Power Loss1} &= (I \cdot I) \cdot R_{ds(on)} \\ &= (2.53 \cdot 2.53) \cdot 0.022 \\ &= 6.4 \cdot 0.022 \\ &= 0.141W \\ \text{Power Loss2} &= (I \cdot I) \cdot R_{ds(on)} \\ &= (0.9 \cdot 0.9) \cdot 0.022 \\ &= 0.81 \cdot 0.022 \\ &= 0.018W \end{aligned}$$



## VCCPLL\_OC



$$\begin{aligned} \text{Power Loss} &= (V_{in} - V_{out}) \cdot I_{out} \\ &= (3.3 - 1.2) \cdot 0.17 \\ &= 2.1 \cdot 0.17 \\ &= 0.357W \end{aligned}$$

$$\begin{aligned} \text{Power Loss} &= (V_{in} - V_{out}) \cdot I_{out} \\ &= (3.3 - 1.2) \cdot 0.25 \\ &= 2.1 \cdot 0.25 \\ &= 0.525W \end{aligned}$$

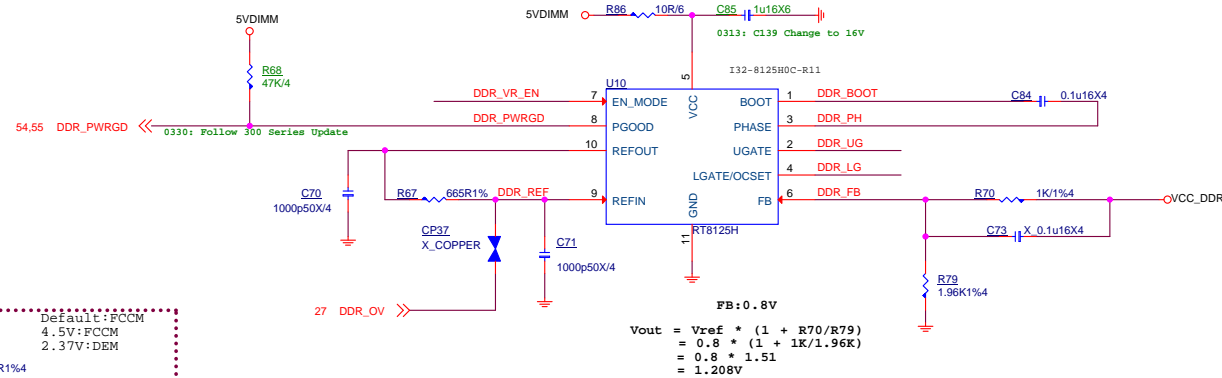
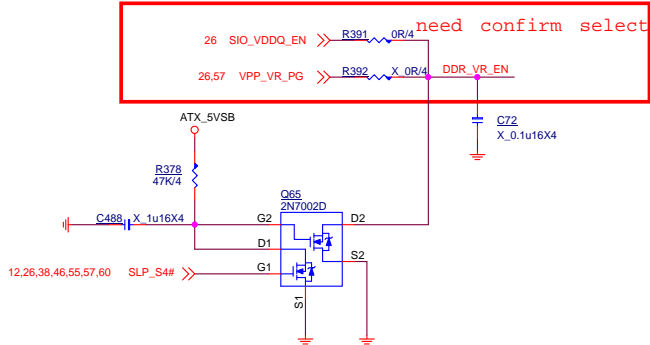
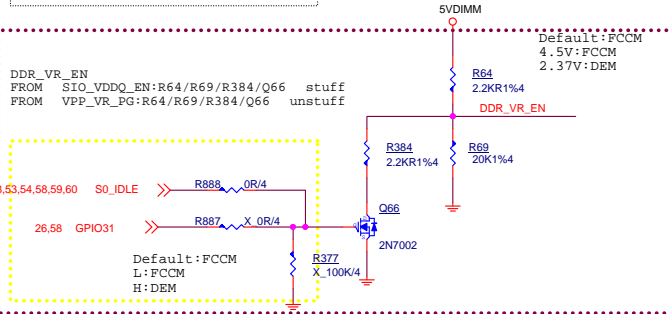
# DDR4 Power:1.2V,13.48A(17.08A)

3.68A For CPU  
9.1A For 4DIMM  
0.7A For DDR VTT

## Choke Isat=18A Test OCP:21A

$I_{ocp} = R_{ocset} * I_{ocset} / R_{dson(LOW)}$   
 $= 7.5K * 10uA / 3.9m$   
 $= 19.23A$   
 $I_{ocp} = R_{ocset} * I_{ocset} / R_{dson(MAX)}$   
 $= 7.5K * 10uA / 5.1m$   
 $= 14.71A$

**Rdson(Low Side) 5V**  
**D03-4503N0C-ST8: 3.9 ~5.1 mohm**

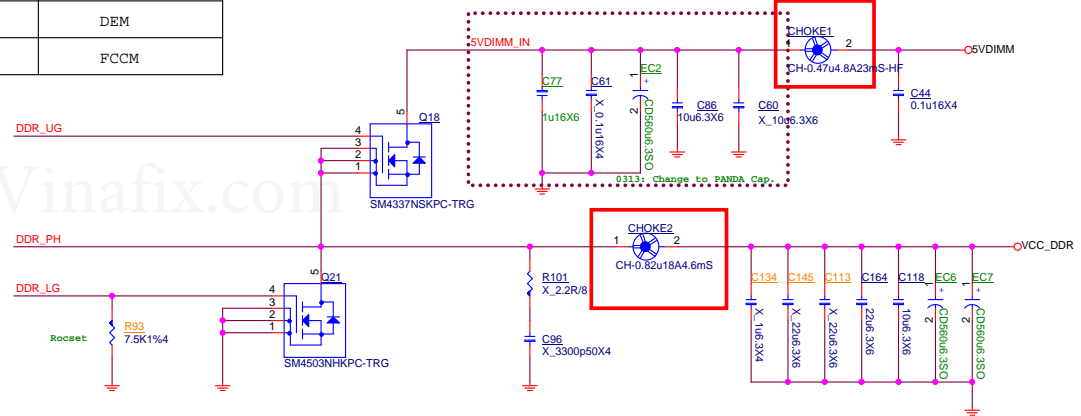


EN_MODE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1~2.7V	DEM
4.3~5V	FCCM

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

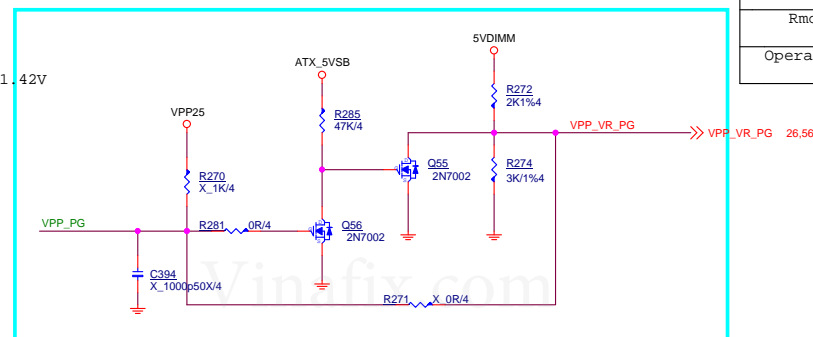
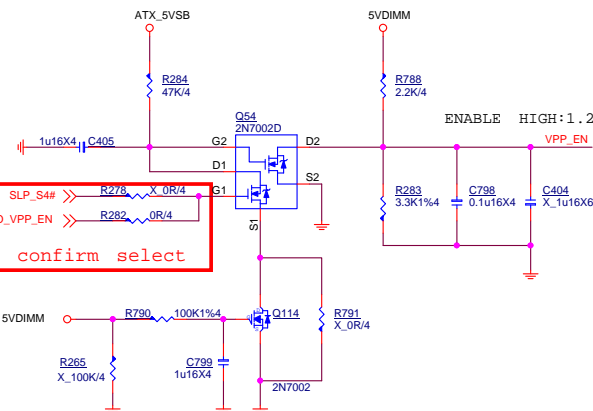
$$= 13.5 * 0.427$$

$$= 5.765A$$



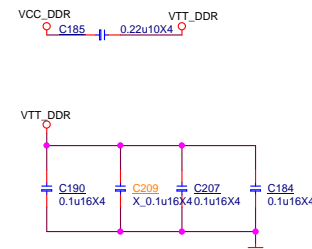
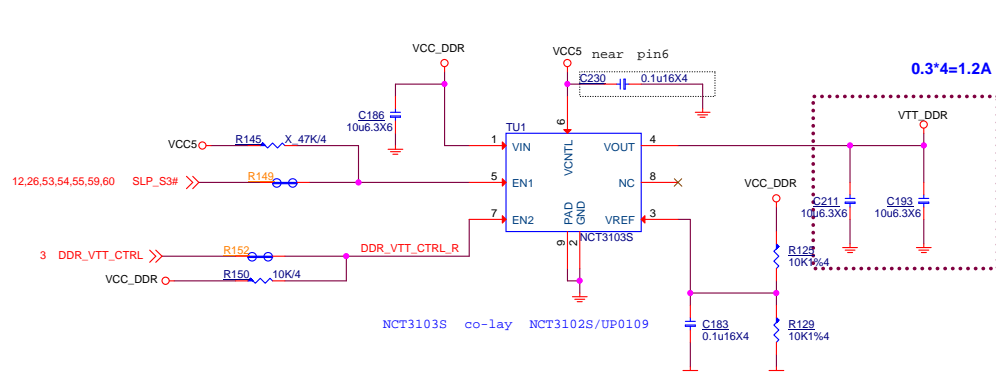
## Test OCP:8.6A

$$\begin{aligned} V_{out} &= V_{ref} \cdot \{(R_{277} + R_{273}) / R_{273}\} \\ &= 0.6 \cdot \{(1K + 0.316K) / 0.316K\} \\ &= 2.499V \end{aligned}$$



Vmode(VPP25_MODE)	0~0.3V	0.3~1.2V	>1.2V
Rmode	0R	100K~150K	To VCC(recommend) or R>400K
Operating Mode	Eco-Mode	Out-Of-Audio	FCCM

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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**MICRO-STAR INT'L CO.,LTD**

**MS-7C75**

Size	Document Description
Custom	<b>DDR PWR VPP25/VT</b>

Rev	1.1
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Date: Friday, December 27, 2019 Sheet 57 of 70

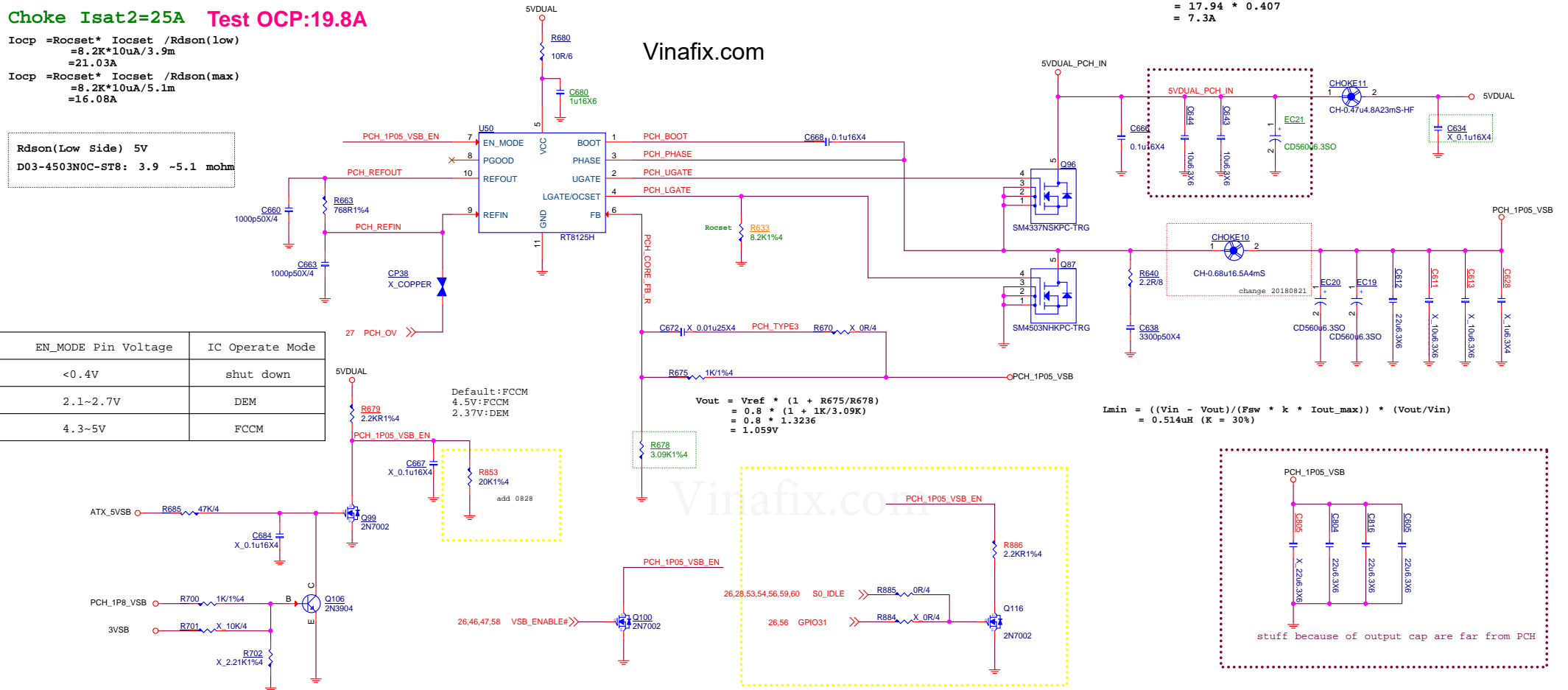
**PCH\_1P05\_VSB Power:1.05V,14.512A+3.43A=17.942A\*80%=14.3536A**

**Choke Isat2=25A Test OCP:19.8A**

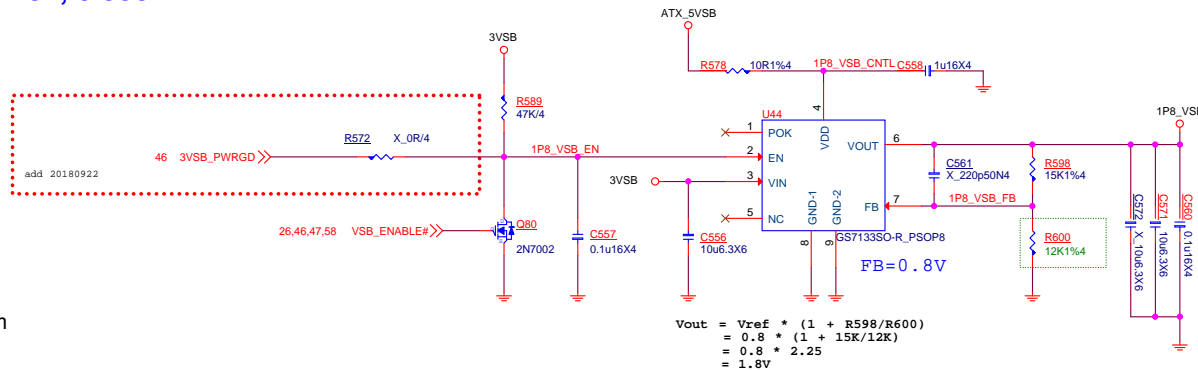
$I_{ocp} = R_{ocset} * I_{ocset} / R_{dson}(low)$   
 $= 8.2K * 10uA / 3.9m$   
 $= 21.03A$   
 $I_{ocp} = R_{ocset} * I_{ocset} / R_{dson}(max)$   
 $= 8.2K * 10uA / 5.1m$   
 $= 16.08A$

**Rdson(Low Side) 5V**  
**D03-4503N0C-ST8: 3.9 -5.1 mohm**

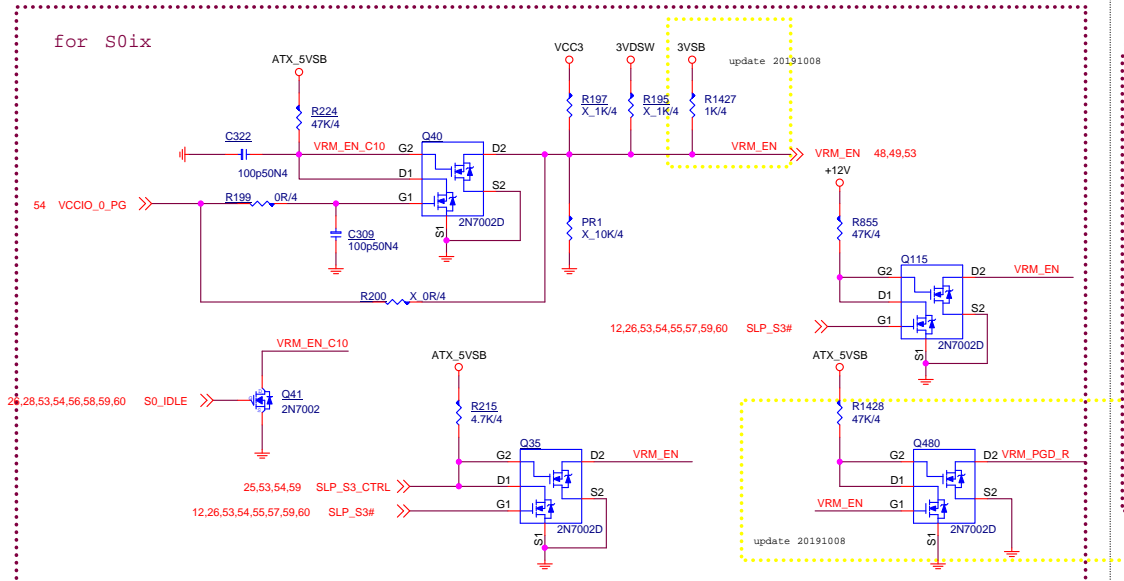
EN_MODE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1~2.7V	DEM
4.3~5V	FCCM



**1P8\_VSB Power:1.8V, 0.358A**

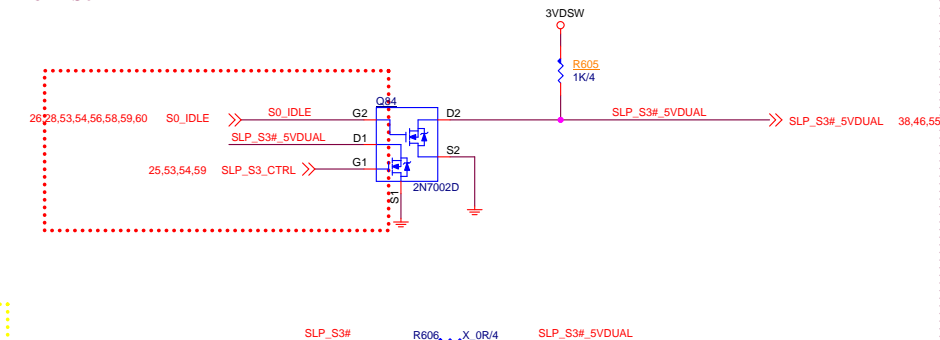


for S0ix

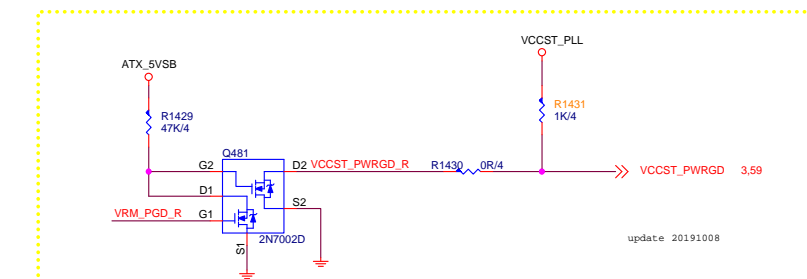
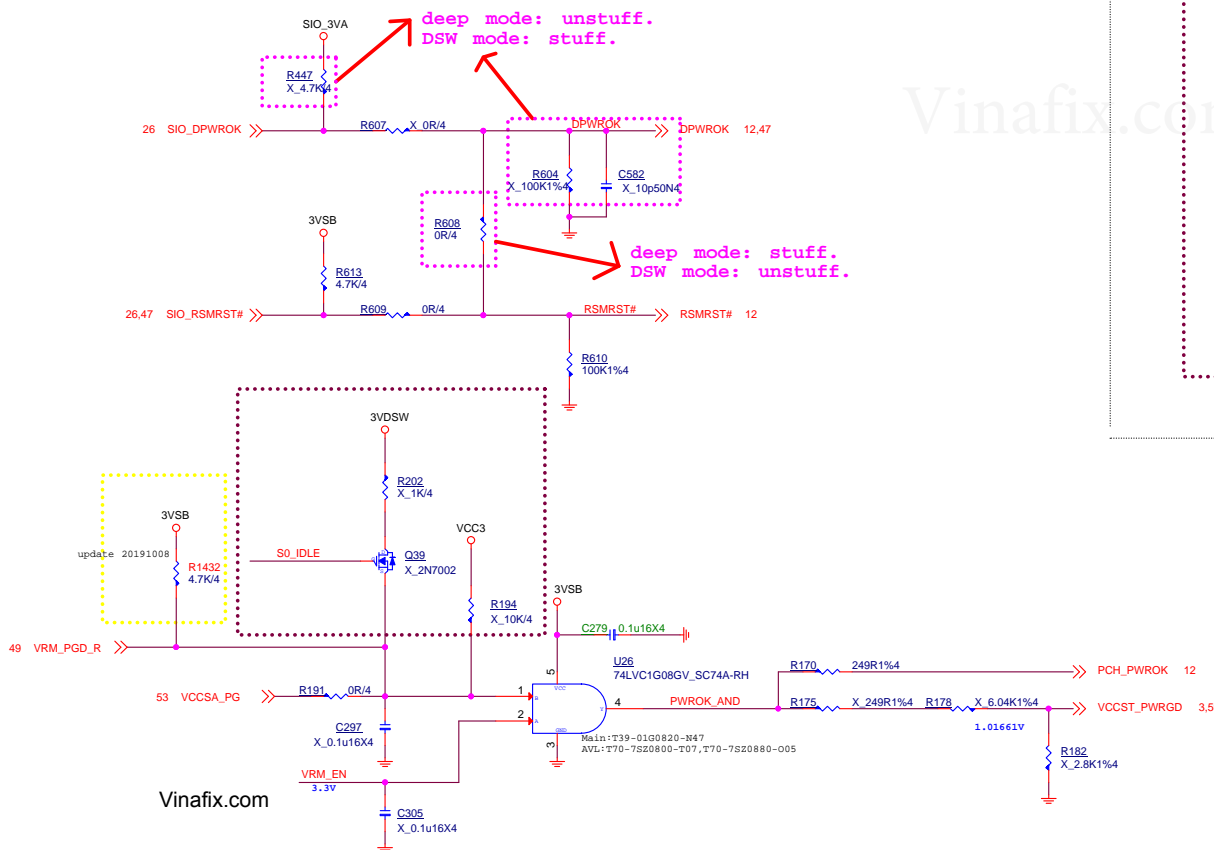
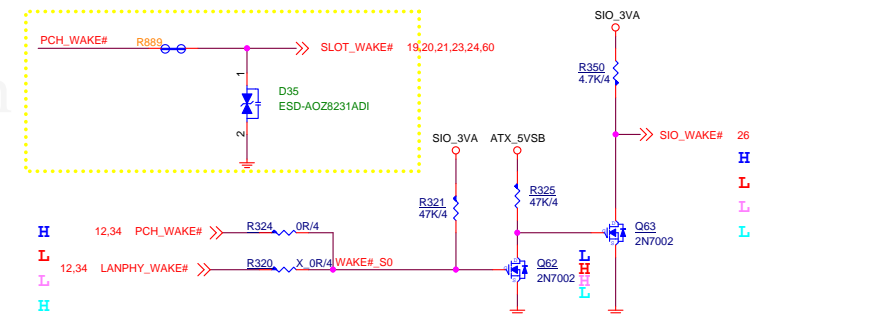


for 5VDIMM and 5VDUAL

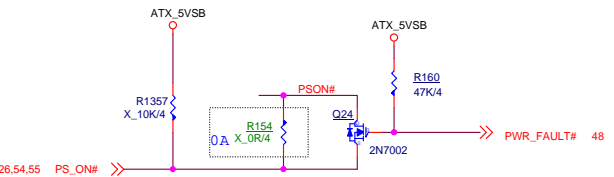
for S0ix



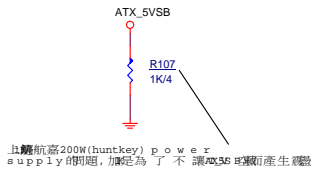
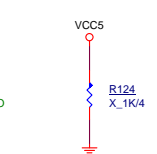
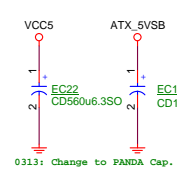
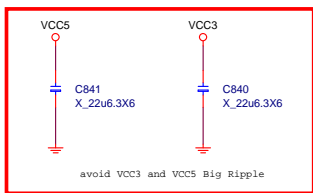
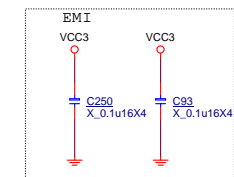
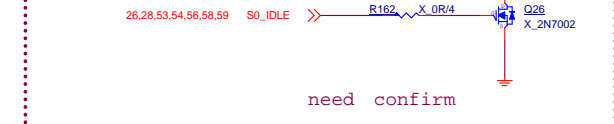
for wake



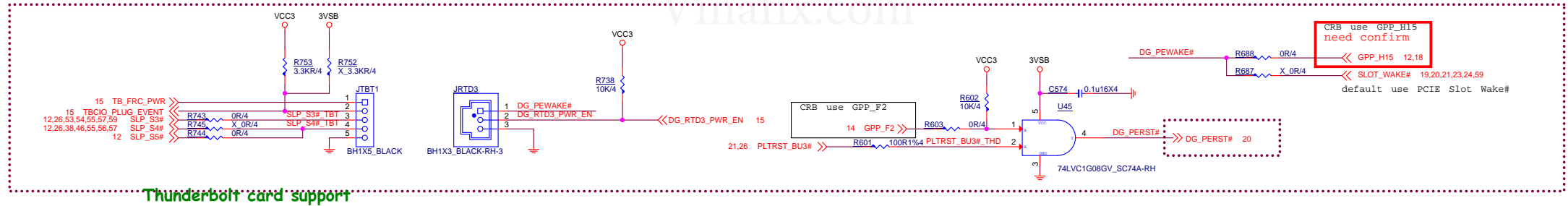
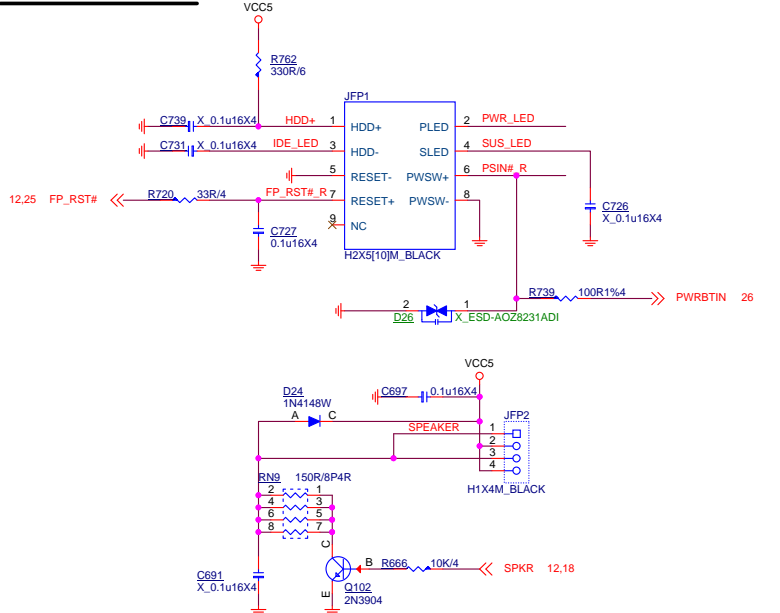
## ATX POWER CONNECTOR



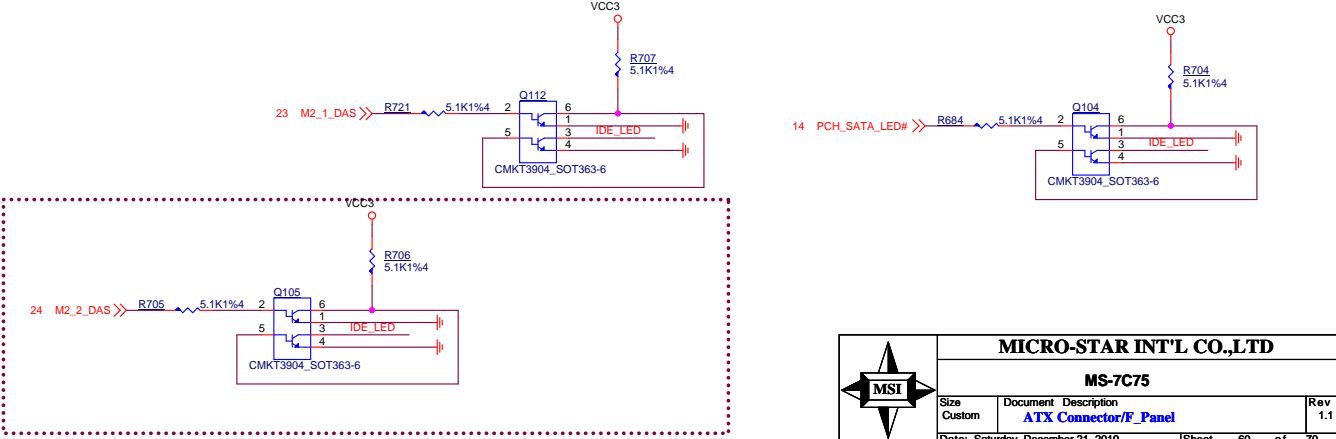
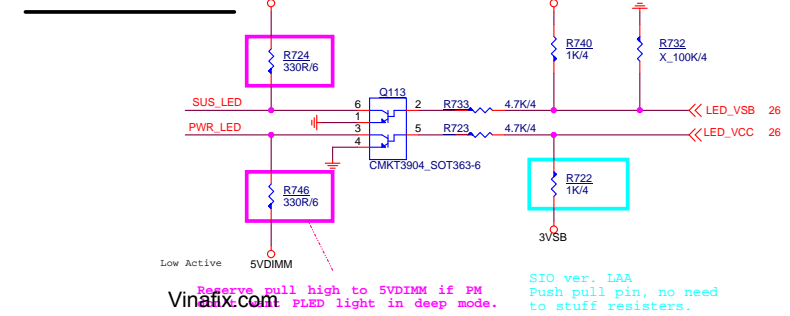
for S0ix



## FRONT PANNEL



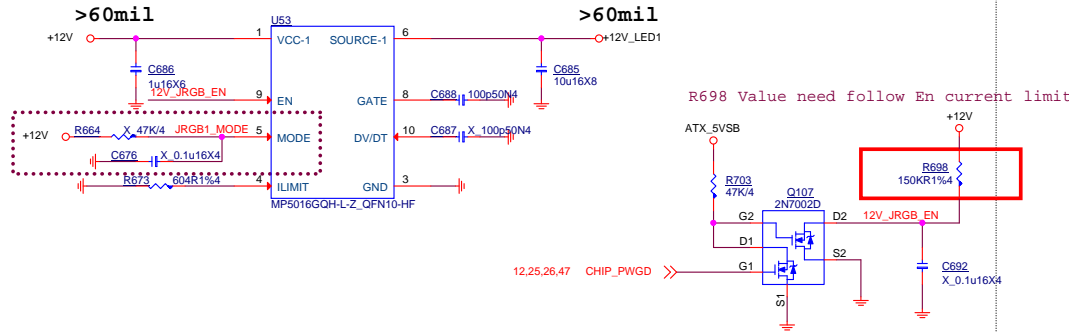
## Front Panel LED



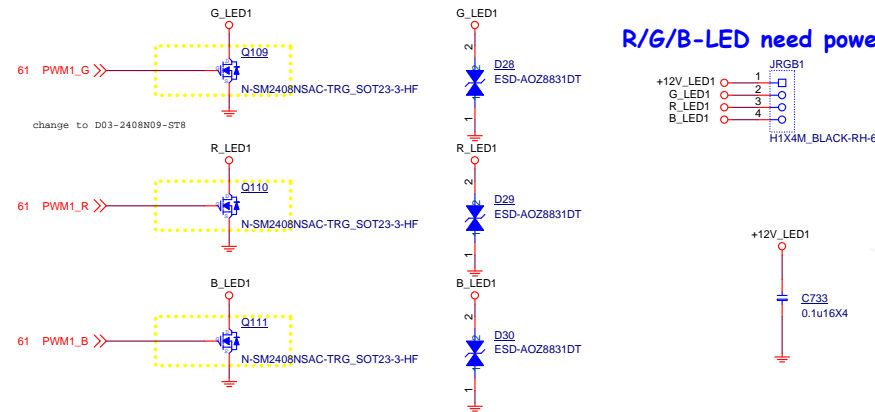




## JRGB1



## R/G/B-LED need power plane



Q109/Q110/Q111 S need power plane and at least 6via.

## Enable (EN)

The MP5016-L is enabled when EN is high. The MP5016-L is disabled when EN is low. Floating EN shuts down the MP5016-L because there is an internal 2.2MΩ resistor pulling EN down to ground. For automatic start-up, connect a pull-up resistor from VCC to EN.

EN is clamped internally using a 5.5V Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to VCC limits the EN input current below 100μA to prevent damage to the Zener diode. For example, when connecting a 300kΩ pull-up resistor to 15V VCC,  $I_{Zener} = (15V - 5.5V) / 300k\Omega - 5.5V / 2.2M\Omega = 29\mu A$ .

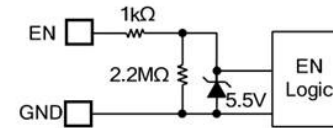
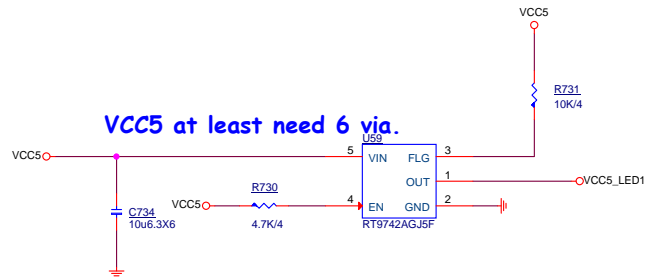
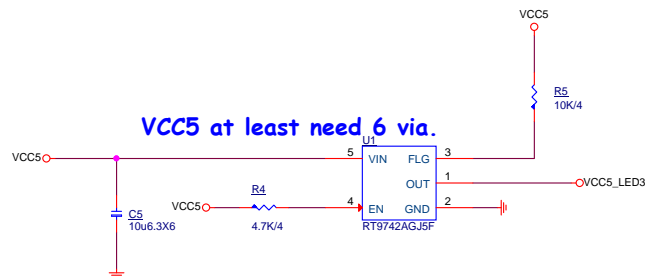
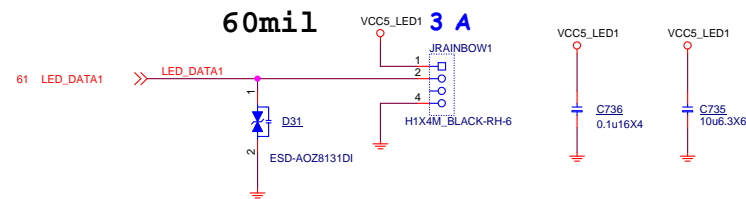


Figure 2: Zener Diode between EN and GND

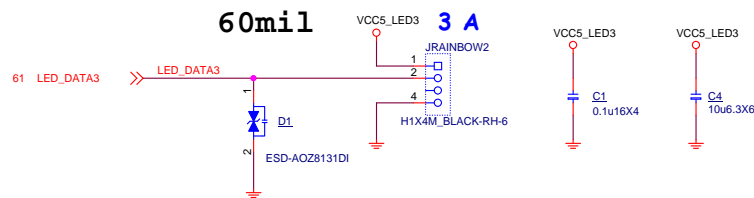
When using a pull-up resistor to set the power-on threshold, avoid using a pull-up resistor that is too small to increase the operational quiescent current.



### JRAINBOW1 LED

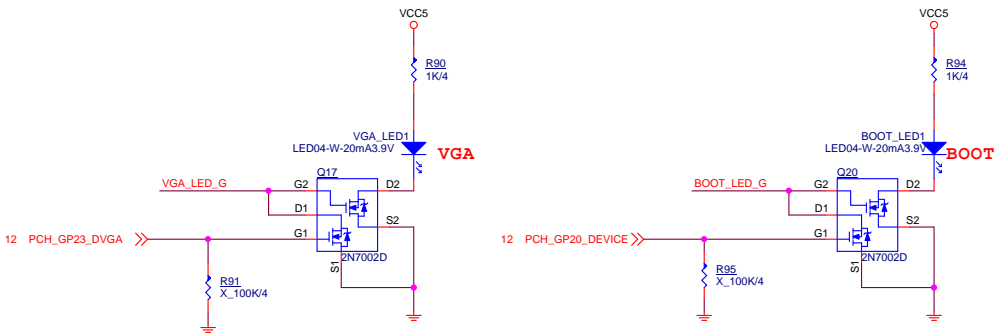
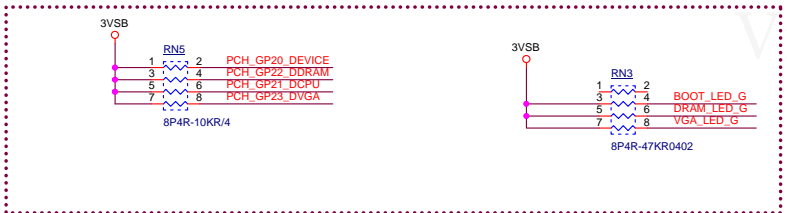
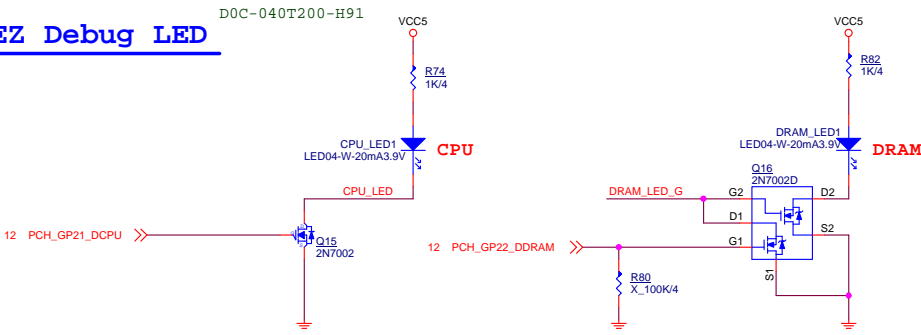


### JRAINBOW2 LED



Vinafix.com

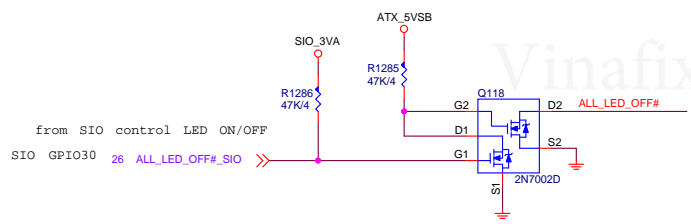
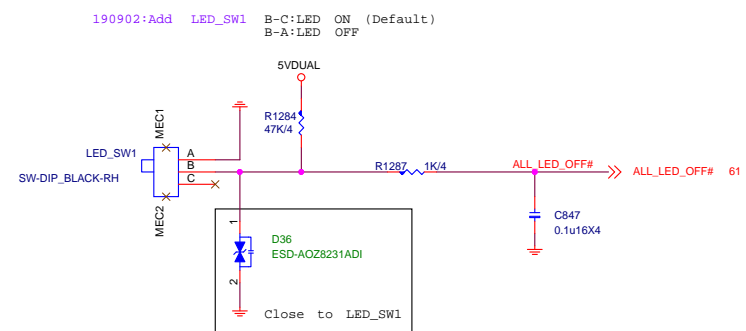
EZ Debug LED



LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

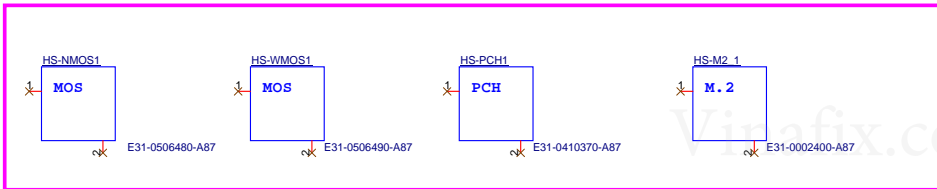
LED  
RED:D0C-040P100-H91  
AVL:D0C-040S500-E07  
  
WHI:D0C-040T200-H91  
AVL:D0C-040S200-E07

開機斷電狀態下，個先維持全暗，開機後  
首先進行亮，後則減掉。  
接著依序進行亮，後則減掉。  
的，後則減掉。  
因此最後正常順利開機後，三個燈都亮。  
(系統重啟或其他原因造成系統重開機則仍按上述操作)

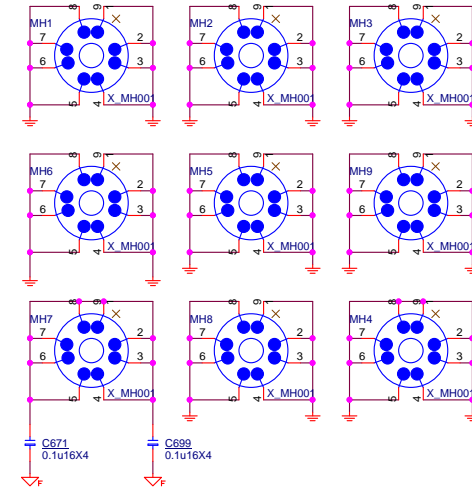




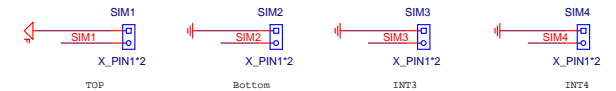
## Heat Sink



## Mounting Holes



## Simulation



## Optical Fiducial Marks-120

